ELECTROMAGNETIC COUPLING IN MULTILAYER THIN-FILM ORGANIC PACKAGES WITH CHIP-LAST EMBEDDED ACTIVES

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ELECTROMAGNETIC COUPLING IN MULTILAYER THIN-FILM ORGANIC PACKAGES WITH CHIP-LAST EMBEDDED ACTIVES

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To my mom, dad, patti and jagan

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SUMMARY

During the last decade, the trend in consumer electronics has been to develop products with better performance, smaller size, lower cost and enhanced functionality. This emerging trend in consumer electronics, referred to as convergent systems, need technologies that can integrate digital, RF, analog and sensor functions with minimal interference. Enhanced multi-functionality in a given form factor requires innovative integration technologies, such as System-on-Chip (SOC), System-in-Package (SIP) and System-on-Package (SOP). Multi-function integration within a single chip is targeted by the SOC approach, while integration at the package level is sought by the SIP and SOP approaches. SIP involves stacking ICs and wire bonding to interconnect each other and SOP aims for total system miniaturization that includes actives, passives, thermal interfaces, power sources as well as packages .SIP and SOP are significantly better than SOC in terms of cost, system complexity and product development time, just to name a few. In order to further system miniaturization, SOP approach has been embedding passive components within the package substrates for some time now. However, sustaining the miniaturization trend requires embedding active chips as well, which is now being actively explored by both academia and industry. Embedding components within the package causes strong unwanted interferences between the digital and analog-radio frequency (RF) sections of the package, which is a major challenge yet to be addressed. Figure 1 shows one such configuration of a multilayer package containing embedded active (digital, analog/RF chips) and passive components. Solving these challenges require a thorough understanding of the underlying

issues with the packaging technology as well as their impact on the system performance in terms of signal distribution and power delivery.

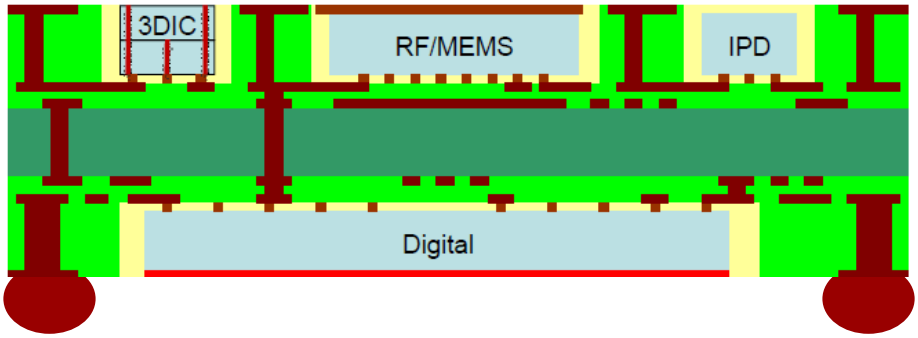


Figure 1 Multilayer system module with embedded chips [1**]**

The objective of this dissertation is to address power integrity problems in packages with active chips embedded within the substrate layers, and to develop solutions for electromagnetic interference and noise coupling. Power integrity is an important system performance driver and it is therefore essential to acquire an in-depth understanding of the issues that impact the power integrity of packages with embedded actives. The predominant challenge encountered with respect to power integrity in mixed signal systems, and especially in the case of multilayer packages with embedded chips, is the electromagnetic coupling through the power distribution network. This dissertation demonstrates various mechanisms of interaction and interference between the embedded chip and the package. Also, the influence of the cavity, formed to embed the chip, on the electromagnetic coupling through the package is studied. Based on the analysis of the package under various configurations, methods are proposed to effectively suppress the propagation of noise both horizontally and vertically through the package. The electromagnetic coupling through the package and the suppression methodology are demonstrated through simulations and measurements for packages with different layer stack-up. The effects of electromagnetic

coupling on the chip embedded within the package are investigated and compared with conventional packaging where chips are surface mounted. In particular, the influence of the package electromagnetic fields on the bulk substrate and the bond-pads of the chip are demonstrated. Finally, the challenges with power integrity in packages with embedded chips are summarized, and guidelines for overcoming them are provided.

This dissertation establishes the important factors that impact the noise coupling at the package level when chips are embedded, develops suitable suppression methodologies to tackle the noise coupling, and demonstrates the factors due to which the chip experiences strong electromagnetic interference when embedded within the substrate cavity. In other words, the dissertation puts forth issues that are foremost in influencing the power integrity of packages with embedded actives, which is crucial to designing efficient power delivery networks.

These are the major contributions of this dissertation:

1. Identification, analysis and demonstration of electromagnetic coupling in multilayer packages with embedded actives.
2. A suppression methodology for electromagnetic coupling in packages with embedded actives, which is effective even in the GHz range of operating frequencies.
3. A novel synthesis method for the coupling suppression technique in (2) that provides noise isolation within the desired frequency bands for multilayer packages.
4. Analysis and demonstration of the impact of electromagnetic coupling on the bond pads and substrate of the chip embedded within the cavity formed in the package.

5. Design guidelines for efficient power distribution in multilayer packages with embedded chips.

CHAPTER 1

INTRODUCTION

Over the past decade, the communication industry has been pushing for a rapid convergence of digital computing and analog wireless technologies. Portable electronics, such as mobile handheld products, netbooks, laptops, personal digital assistants (PDAs) and smart cards are some of the evidences of this convergence. These applications require new packaging technologies that go well beyond the realm of traditional packaging due to the need for even smaller form factors, increased functionalities and reduced costs [**2**] [**3**] [**4**]. Moreover, the high frequency, high I/O density, and low parasitics requirements of these applications have led to new packaging configurations that combine various traditional packaging techniques (e.g., flip-chip and wire-bond, and build-up and laminate substrates) to bring about package-level integration of disparate device functions [**5**] [**6**] [**7**] [**8**]. The optimum solution often lies in a judicious combination, or in other words, the "hybridization" of these seemingly dissimilar technologies and approaches.

Owing to the functional integration needs, semiconductor chip makers have steadily increased the performance of chips by adding functionalities with increasing I/O count and decreasing chip sizes. In this context, we define a system platform, referred to as a System-on-Chip (SOC) that includes both the system hardware (digital and analog/RF) and the embedded software on a single chip. An example of a SOC that combines an INTEL microprocessor with advanced wireless radio, multimedia, and sensor functionalities is shown below in Figure 2 [**9**].

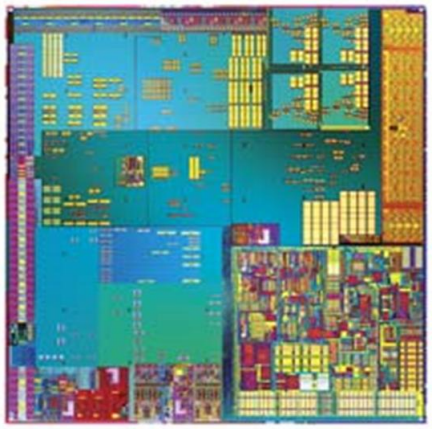


Figure 2 System-On-Chip (Intel)

SOC offers the promise for the most compact and highest performance device that can be mass produced and hence, it has been a part of the roadmap of semiconductor companies for over a decade now. It is important to study the drawbacks associated with SOC as it will help in understanding if this technology can continue producing cost-effective complete end-product systems. Integrating a heterogeneous system on a single chip is by no means a panacea. On standard silicon, a major concern is noise coupling between digital switching circuits and noise-sensitive analog/RF circuits due to the finite resistivity of the silicon substrate [**10**]. Moreover, on-chip noise isolation techniques increase the chip cost. Another major challenge is distributing power to the digital and RF circuits at different voltage levels, while simultaneously maintaining high isolation and low electromagnetic interferences (EMI) [**11**]. Signal transmission on chip is not necessarily faster as the on-chip wire resistance is higher than that for traces on package [**12**]. Hence, the per unit on-chip signal propagation speed (30–70 ps/mm) is slower as compared to the per unit signal speed on package (10–20 ps/mm). Integrating diverse functionalities on chip significantly increases the system costs. In the case of RF/analog

circuit integration in CMOS processes, the fabrication techniques and the technology adaptation further increase the costs involved. Memory integration also becomes expensive as additional processing steps, such as formation of trenches and folded capacitors are required for DRAMS. Embedding logic into memory is not an easy task since DRAM requires lesser number of metal layers [**13**]. Moreover, embedded memories occupy 50–80% of the chip area [**14**], which means that there is really not much benefit in terms of miniaturization with embedded memories. This is going to be an issue with memory intensive SOCs. When integrating passives on chip, the losses associated with the chip substrate affect the performance of the passive components. The Q-factor of on-chip passives is limited to 5–25 due to the inherent losses of silicon [**15**]. Although this can be improved by using thick oxides (e.g., high-resistivity silicon, Silicon–Germanium (SiGe), or Gallium–Arsenide (GaAs)), they inflate the costs substantially. Moreover, passive components consume valuable real estate and occupy more than 50% of the silicon area [**16**]. Other challenges with SOC include long design times due to integration complexities, high wafer fabrication costs, test costs, mixed-signal processing complexities requiring dozens of mask steps, and intellectual property issues [**13**]. Therefore, a new paradigm for overcoming many of the shortcomings of both SOC and traditional packaging technologies has become necessary.

System-on-Package (SOP) and System-in-Package (SIP) technologies seek to overcome many of the drawbacks of SOC through functional integration at the package level rather than at the chip level. The costs involved in realizing package level integration are lesser when compared to SOC. It is shown in [**17**], through different case studies, that multi-chip integration using SOP offers a lower cost solution for high

performance mixed-signal systems as compared to SOC. SIP stacks bare and packaged ICs which are then interconnected using wire-bond assembly technologies on organic or ceramic substrates [**18**]. There are many variations of SIP, which include stacked chips, stacked packages (such as Package-on-Package and Package-in-Package), and chip and package stacked together [**19**]. There is also active research in stacking chips vertically using Through Silicon Via (TSV) technology [**20**] [**21**] as the next step in active IC miniaturization and functional integration at module level. This are referred to as 3D ICs wherein the stacked chips are interconnected, not by wire-bond or flip-chip but by through-silicon-vias (TSVs). However, TSV and 3D chip stacking technologies are still in the emerging phase and are currently higher cost solutions as compared to conventional SIP technologies. In addition, they are quite limited to active ICs only when it comes to addressing heterogeneous system integration, ranging from antenna to baseband components. Figure 3 shows three different configurations of SIP, chips stacked using wire-bonds, chips and packages stacked together and chips stacked using TSVs in that order.

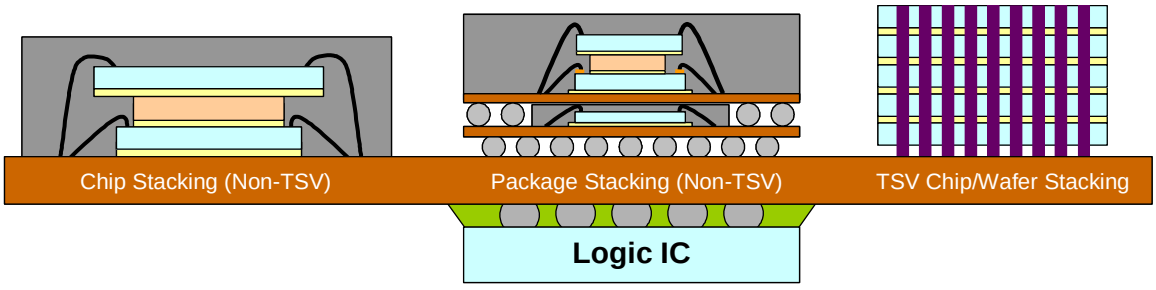


Figure 3 System-In-Package and 3D ICs [18**]**

SOP goes one step beyond SIP and 3D stacked ICs to provide a path for miniaturization at system level. SOP furthers system integration by adding functionality into the package substrate in the form of actives, passives and other system components. Figure 4 shows the functional integration with embedded thin film components [**22**] [**23**]. In SOP, passive devices that are typically mounted on the surface of the board are embedded within the package. The embedded thin film passive components have lesser parasitics as compared to the discrete passives and offer better performance [**24**] [**25**].

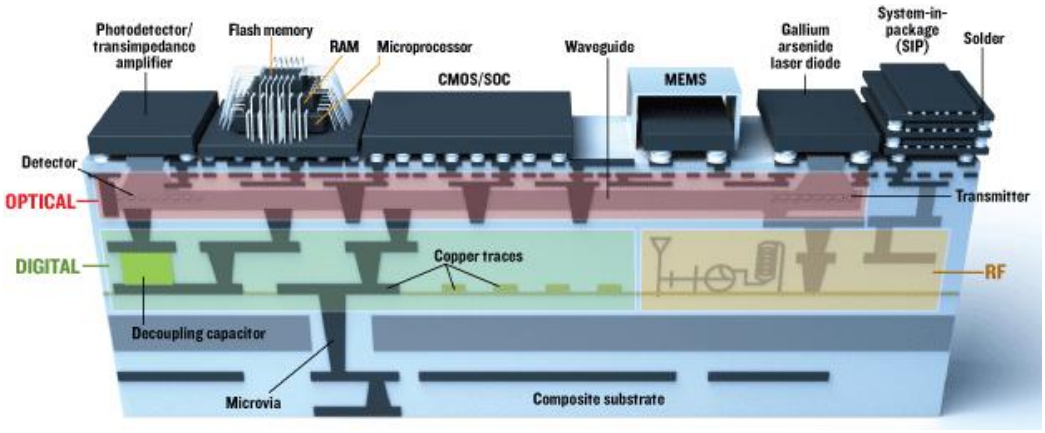


Figure 4 System-On-Package [IEEE Spectrum, June 2006] [22**]**

Embedding passive components within the substrate has been under development for some time now. The relatively newer approach for sustaining the miniaturization trend is to embed active chips within packages, which offers a viable strategy for realizing systems with even smaller and thinner package profiles [**26**]. Figure 5 shows a chip embedded within a cavity in a multilayer package.

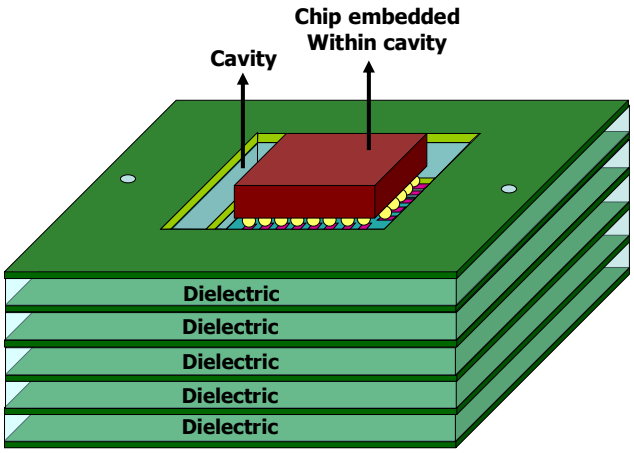


Figure 5 Package with embedded chip

The trend of embedding active chips in substrates has been pursued so far by General Electric [**27**], Intel [**28**], Shinko [**29**], Fraunhofer Institute [**30**], and others. There are two popular approaches to embedding chips within substrates: chip-first and chip-last. The chip-first approach embeds the chip either at the bottom, or in between the build-up dielectric layers, while the wiring layers are formed after the chip has been embedded, as shown in Figure 6 [**31**]. In this approach, the chip assembly can be by direct thin film interconnection to the back-end-of-line (BEOL) of the chip as shown in Figure 7 or in some cases it can be in flip-chip style as in Figure 6. Also, more recently, chips with wafer level fan-out are also being embedded using the chip-first approach, as shown in Figure 8 [**32**]. These technologies are based on either the chips simultaneously mounted on a detachable-tape or molded by a carrier or molding compound, and are interconnected using thin film package wiring processes similar to BEOL. An alternative to this is to mount the chips on rigid-core surfaces and then interconnected using thin-film package processes [**1**].

The chip-last approach, developed by the Packaging Research Center at Georgia Tech, embeds the chip after all the build-up dielectric layers and package wiring have been completed, as shown in Figure 9 [**31**]. In this approach, ultra-thin ICs and passives are embedded in high precision cavity structures on both sides of thin core organic substrates with high I/O density vertical and horizontal interconnections.

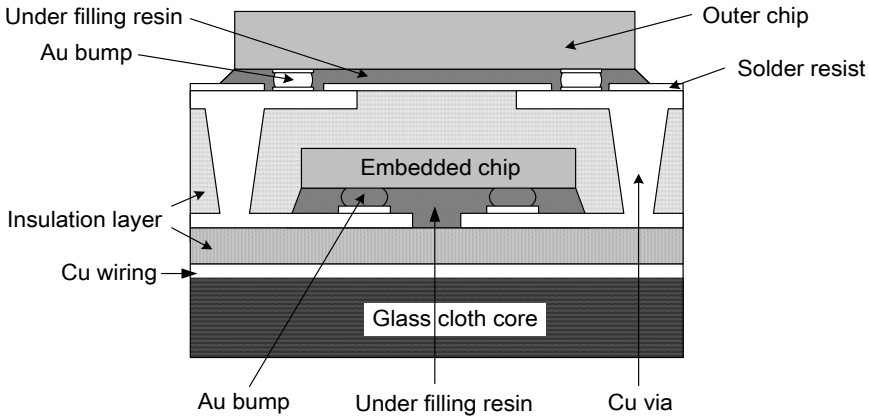


Figure 6 Chip-first embedded chip package - Shinko [29**]**

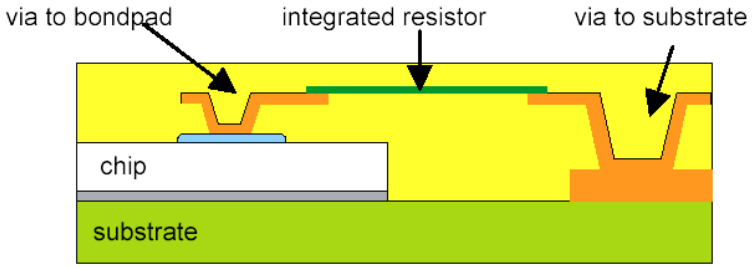


Figure 7 Chip-first embedded chip package -- Fraunhofer IZM [29]

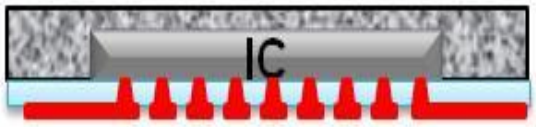


Figure 8 Embedded chip with wafer level fan-out [32**]**

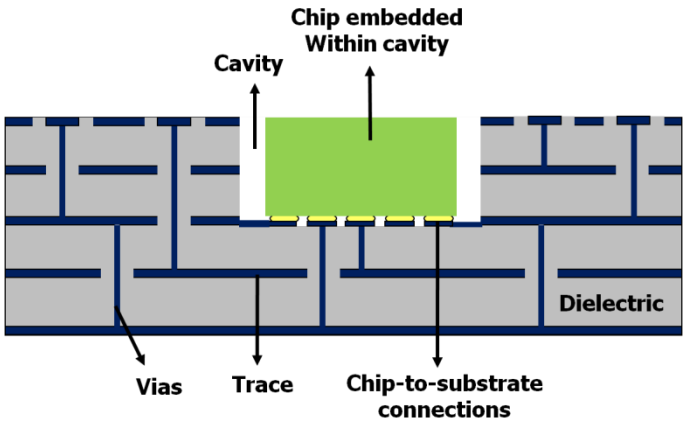


Figure 9 Chip-last embedded chip package

The chip-first approach suffers from the following limitations:

1. The chip is subjected to a lot of processing steps after it is embedded and it can be affected by the fabrication processes
2. Serial chip-to-build-up processes accumulate yield losses that are associated with each process
3. Defective chips cannot be easily reworked thus requiring 100% Known Good Dies (KGDs)
4. The interconnections, which are direct metallurgical contacts, in chip-first approach can result in fatigue failures due to thermal stresses
5. Thermal management issues are also evident since the chip is totally embedded within the polymer material of the substrates, or between build-up layers

The chip-last method relieves the embedded chip off the fabrication stress as the chips are committed in the last step of module fabrication after completion and testing of the substrate with cavity. It allows embedding of chips, Integrated Passive Devices

(IPDs), and discrete passives in different substrates, such as silicon, glass, ceramic and laminates. Moreover, the components can be of different thicknesses as the substrates can have multi-depth cavities. It is easier to provide heat dissipation arrangements for the chip as the back surface of the chip is left exposed [**31**]. Another important advantage of chip-last method is the high density interconnections that can be achieved in this approach. The pad to pad interconnections are formed under low temperature bonding and they have a high density with very tight pitches down to 30 um. The interconnect density realized, matches that achieved in the on-chip redistribution layer very well. Also, the reliability of these interconnects can be well characterized since the chip assembly is the last step in the fabrication of the package [**33**] [**34**]. Thus, the chip-last method overcomes most of the challenges associated with the physical structure of chip-first embedded chip package.

The next few paragraphs discuss the advantages offered by chip-last embedded chip packages in terms of functionality, performance and form factor. Commonly used chip assembly schemes in SIP and SOP integration technologies include wire-bond and flip-chip [**35**] [**36**] [**37**]. Some of the significant advantages that flip-chip assembly technology provides over wire-bonds include [**38**] [**39**] [**40**]:

1. **Increased functionality in a smaller die:** Entire surface area of the die is available for die bump placement to connect to a carrier, which eliminates the wire-bond restriction of having all of the pads at the periphery of the chip.
2. **Improved power supply noise performance:** Significantly lower loop inductance is achieved due to an order of magnitude reduction in chip-to-substrate connection length. Also, power can be supplied right where it is required instead

of being routed towards the edge of the die and then brought in towards the core or I/O circuitry as in wire-bond packages.

3. **Superior signal integrity performance:** High impedance nature of the wire-bonds creates impedance discontinuities in fast-switching environments, degrading the signal integrity performance. Wire-bonds also suffer from considerably larger signal-to-signal crosstalk. These phenomenon are significantly mitigated in flip-chip interconnects with controlled impedance lines and smaller signal-to-signal crosstalk.
4. **Reduced package footprint:** Potential reduction in package size as Flip-Chip Ball Grid Array (FCBGA) packages, unlike wire-bond packages, do not require a keep-out area for connecting to the carrier.

Embedding active chips within the substrates provides the advantages of flip-chip packages and aims to further improve the electrical performance of flip-chip packages by reducing the length of package wiring as well as interconnection length between chip and package. In flip-chip and wire-bond configurations, signal and power supply connections from the chip that travel through the package, require through package vias. Embedding the chip within the substrate reduces the number of through package vias and brings the chip electrically closer to the system board. This helps in reducing the overall thickness of the package by making it desirable for mobile phone applications, where there is always a drive for low Z-direction profiles. Reduction in the length of package wiring and vias provides improvement in power supply noise performance as noise voltage across the chip’s power and ground supply is proportional to the impedance of the power

supply loop through the package. Note that impedance is a function of the loop inductance of the package power and ground connections, which increases with a larger loop area. Crosstalk noise from an aggressor pin to a victim pin in a FCBGA package is predominantly inductive in nature and is caused by the overlap of the victim signal-return loop and aggressor signal-return loop. With reduction in the loop area overlap, crosstalk noise can be decreased as well.

Figure 10 shows a package with a surface mount chip, and Figure 11 shows a package with an embedded chip. The area surrounding the embedded chip can be used for signal routing and power/ground supply. As seen from Figure 10 and Figure 11, the package with embedded chip offers reduction in module thickness and signal lines through the package can potentially be shorter as compared to conventional packages. Notice that even though the packages shown in Figure 10 and Figure 11 have the same substrate thickness, surface mounting the chip (Figure 10) results in increased thickness as compared to embedding the chip (Figure 11). Apart from the form factor reduction for a single chip package, embedding chips provides increased functionality within a given package size as shown in Figure 12.

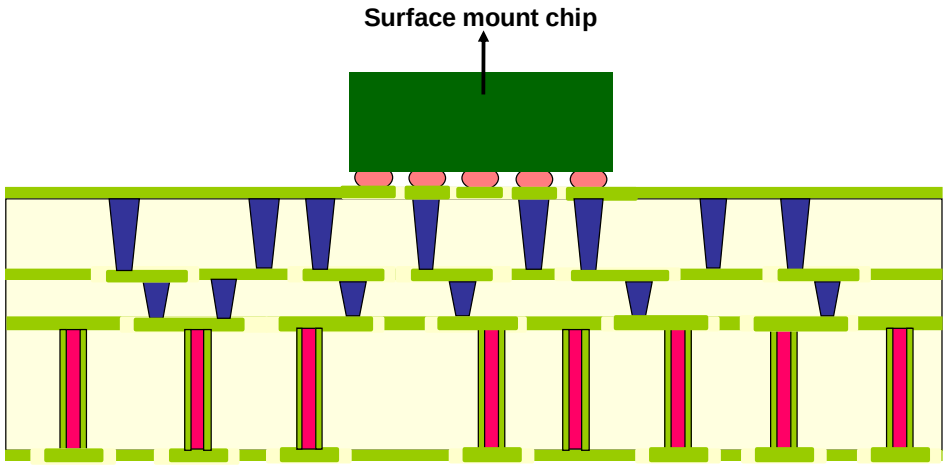


Figure 10 Cross-section of package with surface mount flip-chip

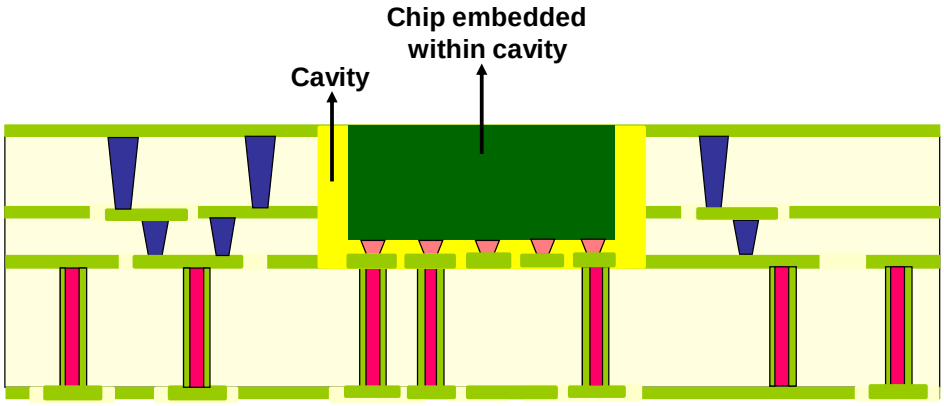


Figure 11 Cross-section of package with chip-last embedded chip

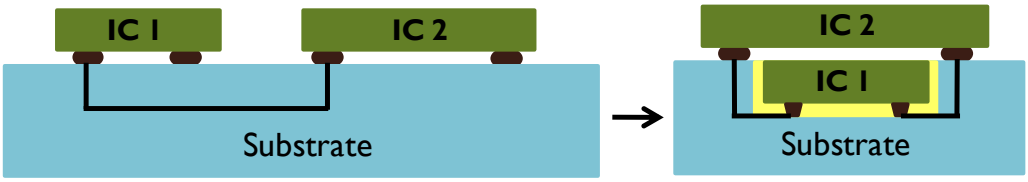


Figure 12 Increase in functionality with smaller package size as benefit of chip-last embedding

Package integration technologies, such as SIP and SOP, have demonstrated how efficient packaging can improve a system's performance, while controlling costs from becoming exorbitant, which is one the main drawbacks in developing SOC solutions. But note that the SIP and SOP methods also increase the system complexity in comparison to conventional packages as multiple dissimilar chips are embedded within the same package in close proximity. Moreover, the substrate is no longer just a supporting platform as it now has functionality in the form of embedded components [**18**]. In the Chip-Last method of embedding active chips, cavities are formed in the dielectric materials to accommodate the chip. The formation of cavities in the package can cause unwanted strong interferences between the digital and analog-RF sections of the package. Parasitic interactions between the different sections of the package can result in global coupling across the package in the form simultaneous switching noise (SSN). The SSN that gets transmitted across the package couples to the power distribution network (PDN) and the signal distribution network (SDN), which is very undesirable. So, packages have to be carefully designed and analyzed in order to ensure the system's overall signal and power integrity [**41**] [**42**].

The system design issues along with power and signal integrity of SIP and SOP systems have been dealt with extensively in literature. This paragraph briefly reviews some of the related work. In [**43**], a method to provide noise isolation in RF-digital SOP using segmented power bus structure is proposed. In [**19**], SIP co-design challenges including the system's I/O requirements and power and signal integrity constraints with respect to different stacking configurations are discussed. An integral analysis technique for signal and power integrity of SIP and SOP is described in [**44**]. In [**45**], the effects of

inductive and capacitive crosstalk, SSN and harmonic interferences in SIP packages using electrical parameters extracted from the layout of a SIP package are analyzed. The electromagnetic interference (EMI) behavior of SIP is analyzed in comparison with that of a discrete system in [**46**]. In particular, the SIP and the system packaged conventionally with discrete components consist of a micro-controller, NAND flash memory and SDRAM memory chips. The individual chips are stacked and mounted on a single substrate in the SIP configuration. The size of the package and the power bouncing noise are both shown to be lesser in SIP when compared to the discrete system in [**46**]. Design challenges for SIP and SOC, and the factors that are important for electrical performance, such as ESD protection for I/Os, drive strength of off-chip buses, capacitive coupling and parasitic inductance effects from bond wires and die attach methods are explored in [**47**]. In [**48**], crosstalk characterization for 3D SIP is discussed. An overview of substrate technology including embedded passives within the substrate layers, chip to substrate connections and memory integration using SIP technology for mobile phone applications are discussed in [**49**]. EMI issues for SOP systems with integrated high-performance digital ICs and RF-analog circuits are explored in [**50**]. Furthermore, the performance benefits obtained in terms of power and signal by using SOP are also evaluated.

In the case of embedded actives, most existing work has mainly dealt with material and process technologies. There has not been much focus on electrical design aspects such as power and signal integrity. It is very essential to acquire an in-depth understanding of the issues that impact the power and signal integrity of packages with embedded actives in order to achieve good system performance. While the design of a

power delivery scheme is specific to each system, its functions, applications and issues with the power network largely depend on the type of packaging used [**51**]. Note that power integrity concerns itself with the proper delivery of power to the IC buffers while ensuring good quality signals. The basic requirements for a power distribution network (PDN) include resonance free impedance profile, uniform stress distribution across the PDN, maintaining the voltage fluctuation due to the transient noise caused by driver switching within the tolerance limit, and providing adequate isolation for electromagnetic interference across the various modules of the package that are supplied power by the PDN. This dissertation focuses on the factors that impact the power integrity of embedded actives.

1.1. Previous Research on Electromagnetic Coupling in Multilayer Packages

Power ground planes which form the power distribution network in a package behave as parallel plate cavity resonators. When a driver switches and its vertical interconnect, called via, penetrates the power and ground plane pair, a current source is setup in the parallel plate cavity due to accumulation of opposite charges on the power and ground planes [**52**]. The current source generates electromagnetic waves which get transmitted through the cavity and encounter multiple reflections at the edges of the planes. Electromagnetic wave propagation through the cavity excites the cavity resonances and causes unwanted interference with victim circuits that are powered by the same power and ground plane pair. When multiple fast switching drivers simultaneously excite the cavity, the unwanted interference is more severe and appears as large voltage fluctuations at victim circuits. This noise is called simultaneous switching noise (SSN)

[**53**]. SSN propagates through the plane pair cavities and causes interference with circuits which are not excited. However, noise propagation in a multilayer package occurs not only in the horizontal direction but also in the vertical direction when there are apertures in the planes forming the parallel plate cavities.

The power/ground planes in multilayer packages have apertures which are created due to the formation of voltage islands for providing isolation among digital, analog and RF sections and due to groups of closely spaced vias, or through holes. Additionally, there may also be other slots created for mounting devices and connectors [**54**]. Figure 13 shows a multilayer stack-up with slots and via holes.

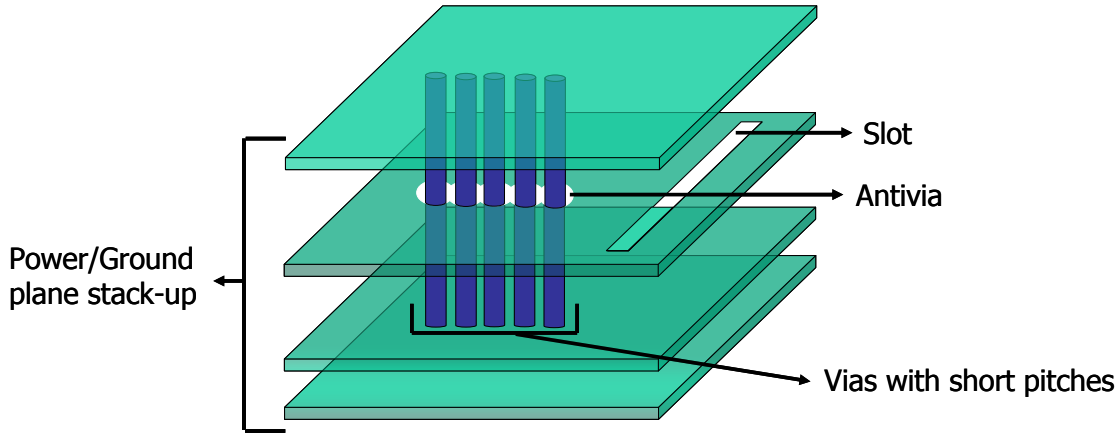


Figure 13 Multilayer Power/Ground plane pair structure

When active chips are embedded within the substrates by chip-last method, cavities are formed in the dielectric layers and apertures are formed in the metal layers of the substrates to house the chips as shown in Figure 14. The presence of the die within the cavity can result in apertures in successive metal layers depending on the thickness of the die. The apertures cause significant coupling of electromagnetic fields across different plane pair cavities [**55**]. The SSN produced also gets transmitted by the electromagnetic

wave propagation to neighboring plane pair cavities. This noise is referred to as vertical-SSN, and it affects the performance of multilayer packages [**56**]. When there are apertures of the same size on successive metal layers in multilayer packages, the coupling across the multiple layers is caused by fringing fields at the plane edges [**57**].

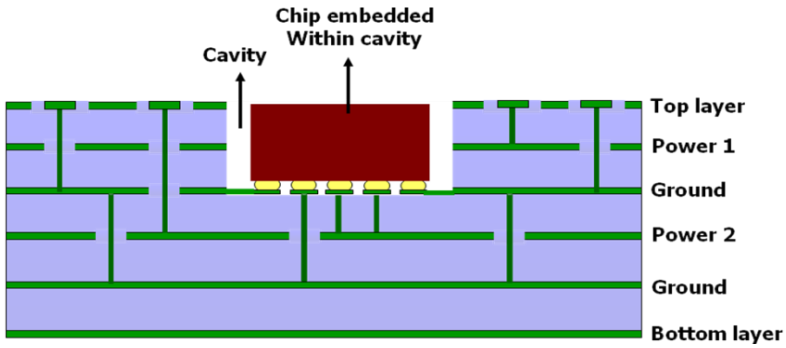


Figure 14 Multilayer package with embedded chip

The dissertation analyzes the effect of vertical electromagnetic coupling in packages with dielectric cavities to embed chips, demonstrates the coupling in packages with different layer stack-up through simulations and measurements from test vehicles and discusses the factors that influence the coupling.

1.2. Previous Research on Suppression of Electromagnetic Coupling in Packages

SSN is detrimental to the power integrity of the system because voltage fluctuations can cause logic errors and false switching of digital circuits [**58**] and degrade signal to noise ratio of RF and analog circuits [**59**]. In the past, various noise suppression techniques have been developed to tackle the noise coupling. These techniques include split planes [**60**], ferrite beads [**61**], decoupling capacitors [**62**] (surface-mount and embedded) and Electromagnetic Band-Gap (EBG) structures [**63**]. These methods are

aimed at tackling the noise coupling problem within a single plane pair cavity. Among these methods, which are popularly used for the suppression of SSN, decoupling capacitors have been used to provide vertical-SSN suppression across different layers in multilayer packages and in packages with split planes, as shown in Figure 15 [**64**]. But this method loses its efficiency as the frequency of operation moves into GHz range. The Equivalent Series Inductance (ESL) of the capacitor and the inductance associated with the capacitor mounting pads and leads influence the frequency limit up to which the capacitor can provide noise suppression. The effective inductance of thin film embedded capacitors is lesser as compared to discrete decoupling capacitors and their usable frequency range is above that of discrete capacitors, yet, they cannot sustain their effectiveness as the frequency of operation moves beyond 2.0 GHz [**65**].

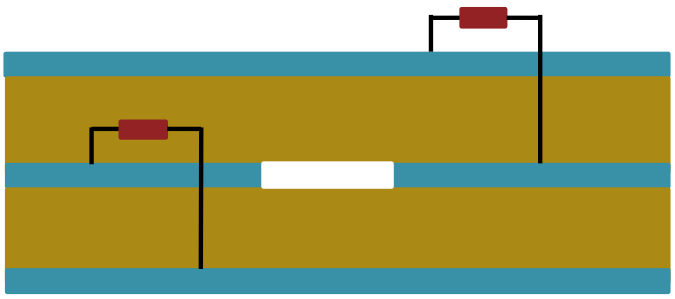


Figure 15 Decoupling capacitors - connected across multiple plane cavities

Another method is proposed in [**66**] to provide suppression of coupling through cutouts and apertures in multilayer substrates by optimally positioning the chip on the package, such that some of the cavity modes get cancelled out and the corresponding resonant peaks get suppressed, as shown in Figure 16. The resonant modes that get excited in a power-ground plane pair cavity depend on the physical location of the source excitation. By changing the chip location, the source excitation location is changed and the cavity

modes which get excited can be manipulated. Also in the approach of [**66**], the size of the package can be changed so that the resonant frequencies of the package are not within the frequency range of the operating chip, as shown in Figure 17. This concept is effective, but to achieve noise suppression either the chip location or the package size needs to be changed. If the system design does not allow this flexibility, this method as described in [**66**] cannot be implemented. Additionally if there are multiple ports (source excitations), it might be harder to achieve optimal chip placement solution for noise suppression.

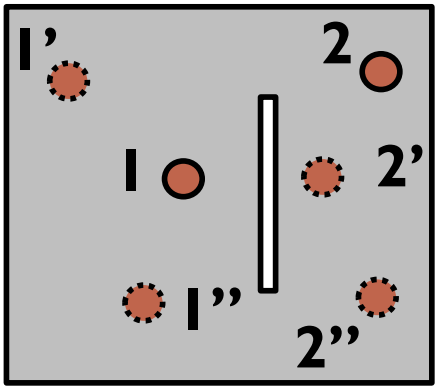


Figure 16 Port locations (1 and 2) modified to suppress unwanted resonances

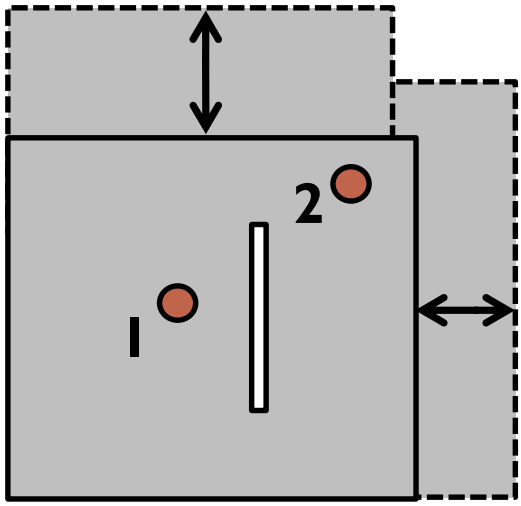


Figure 17 Plane sizes altered to avoid unwanted resonances

The drawbacks of noise coupling through apertures in multilayer packages still persist. The cavities formed in substrates due to embedding chips, as previously shown in Figure 5, are larger than those caused by vias and connector holes and such large cavities/apertures result in significant vertical coupling of electromagnetic fields [**55**]. Therefore, it is necessary to develop effective methods to suppress GHz noise propagation through large apertures formed to embed active chips within multilayer packages.

In this dissertation, suppression of vertical electromagnetic coupling across multiple plane pair cavities is proposed. The proposed methodology uses planar EBG structures to achieve the suppression of vertical electromagnetic coupling. This dissertation discusses design methodology, simulation and measurement results from various multilayer structures to substantiate this method for the design of SOP-based systems operating in GHz range. Furthermore, the influence of apertures and port locations on the vertical coupling is investigated.

1.3. Previous Research on the Effect of Package Parasitics and Electromagnetic Fields on Surface Mounted Chips

An advantage to embedding chips within substrates is that the packages are thinner than those with surface mounted chips. However, as mentioned in Section 1.1, this is true only if the packaging makes use of the area surrounding the chip for routing signal and power/ground supplies. In chip-last method, the chip is embedded in flip-chip style to keep the parasitics of the chip to the substrate connections as low as possible. Figure 18 shows the layers surrounding the chip used for power and ground supplies,

while Figure 19 shows the same layers being used for signal routing. Based on the package configuration, it may be more appropriate to use the metallization layers surrounding the chip either for power/ground supply or for signal routing. In Figure 18, the power/ground layers are marked as P/G. In Figure 19, the layers surrounding the chip are used for signal routing. In some cases, for example in a single chip package as shown in Figure 19, the signal line lengths can increase if they are drawn to the metallization layers surrounding the chip before being taken to the package output terminals (circled in red). So, the layers surrounding the chip should be used appropriately depending on the package configuration without affecting the performance. If the layers surrounding the chip are left unused, as in Figure 20, the embedded actives package may not provide significant advantages, in terms of size over the surface mount packages. This means that it is essential to study and model the interaction of the chip and the package, as well as the noise coupling effects they have on each other. The following paragraphs discuss the chip-package interaction mechanisms in conventional packages with surface mounted chips from various literatures.

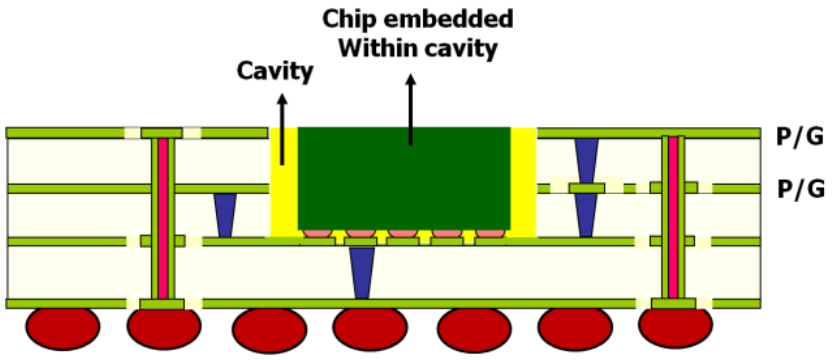


Figure 18 Layers surrounding the embedded chip are used as power-ground supply

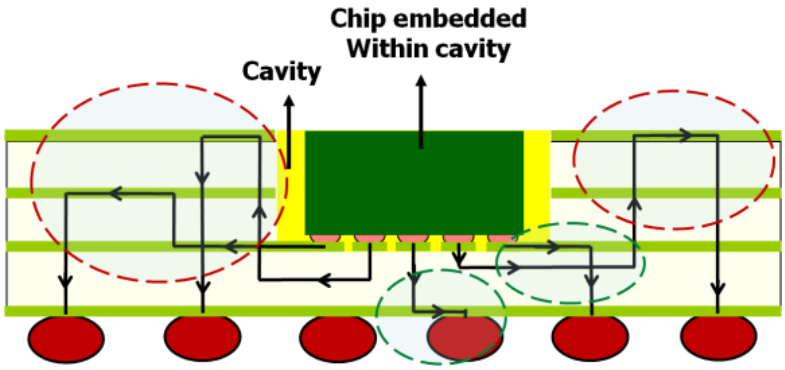


Figure 19 Layers surrounding the embedded chip are used for signal distribution

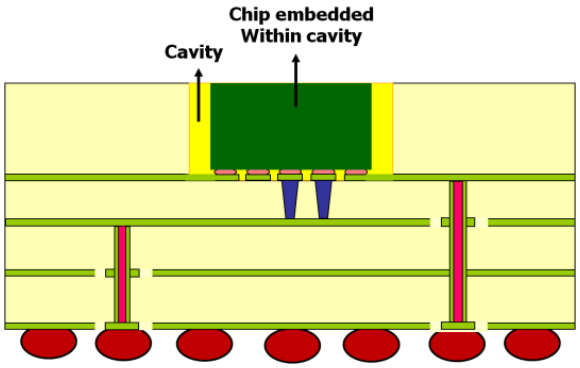


Figure 20 Surrounding metal layers not used in this configuration

On-chip noise and noise generated in the package have so far been analyzed in a decoupled manner [**67**]. On-chip noise coupling through the silicon substrate has always been a major concern for mixed-signal ICs [**68**]. The on-chip substrate coupling is generally analyzed with respect to the influence of on-chip power distribution network (PDN), effect of the parasitics associated with the chip to substrate connections and back metallization of the chip.

The parasitics associated with chip to substrate connections influence the on-chip power-ground noise [**69**]. Parameters of the package (e.g., bond-wire, pin parasitic resistance, etc.) severely affect the stability of bias voltages. In particular, the

bond-wire and pin parasitic resistance, inductance, and capacitance all constitute a Resistor-Inductor-Capacitor (RLC) network which can cause the internal supply voltages to be significantly different from external voltages [**70**]. In addition to this, cross-capacitance and mutual inductance between bond-wires can cause electromagnetic coupling between digital and analog supplies, as shown in Figure 21[**71**]. Therefore, the advantage of Kelvin ground for substrate bias vanishes as disturbances due to digital switching currents propagate through the mutual inductances and cross capacitances. When using flip-chip attached chips, the parasitic effects are lesser as compared to those using wire-bonds. The effects of both capacitive and inductive coupling between bond wires have been analyzed with a TQFP64 (Thin Quad Flat) package in [**72**].

In [**73**], it has been shown through experimental results that flip-chip assembly technique has a much reduced effect on the on-chip supply voltage levels and the fluctuations in the voltages are lesser as compared to wire-bond connections. A test chip designed in 0.18 um CMOS technology is mounted in two different ways, namely — JLCC package and flip-chip assembly technique in order to compare the effect of the assembly techniques on digital switching noise. Chip-in-package and chip-on-board technologies are compared in [**74**], which shows that the chip-on-board technique has better performance owing to the elimination of package parasitics as the chip is directly mounted on the board. In [**75**], chip-in-package and flip-chip are compared, and flip-chip technique is shown to perform better when compared to chip-in-package.

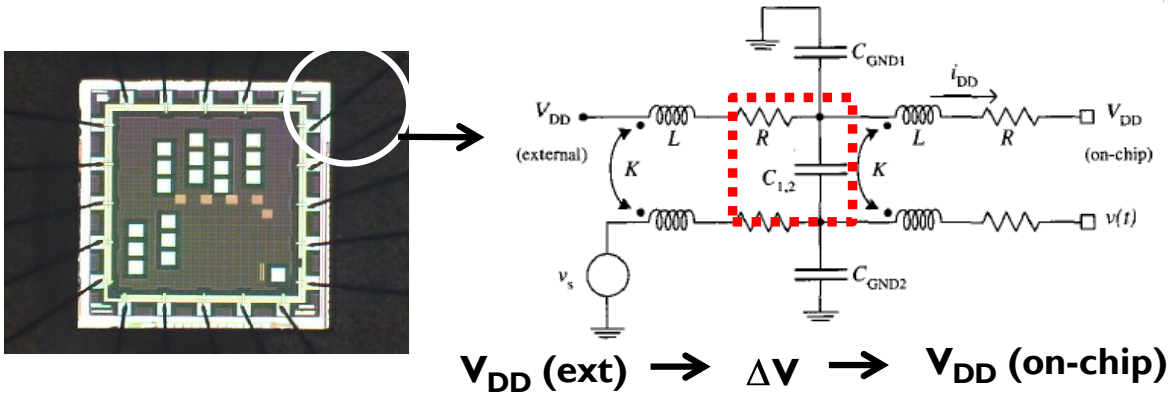


Figure 21 Wire-bonded chip with circuit representation of self and mutual parasitics between bond wires

Another important factor that can influence the on-chip switching noise is the back metallization of the chip. In [**69**], the effect of inductive parasitics in the chip substrate ground network on the bulk currents flowing through the chip substrate, are discussed, as shown in Figure 22. Back side metallization, in some cases, can also result in propagation of parallel plate modes through the chip substrate that interferes with the on-chip circuits. In [**76**], the performance of conventionally packaged GaAs ICs with wire-bonds and flip-chip are compared. In the configuration with wire-bond, the chip is mounted on a metalized surface, which results in power leakage into surface waves with high interconnection losses. Flip-chip technology can be used to reduce, or even avoid surface wave leakage. The effects of using a dielectric carrier substrate as an intermediate platform between the chip and the package substrate are demonstrated in [**77**]. It is shown that the dielectric substrate helps in reducing the parallel plate modes, thereby suppressing surface wave leakage for thinned chips as compared to chips with semiconductor substrate of thickness over 600 um. The effects of having a floating

ground plane on the backside of a flip-chip mounted IC are discussed in [**78**]. The floating ground plane can form a parallel plate wave guide in association with package metallization layers and increase surface wave leakage.

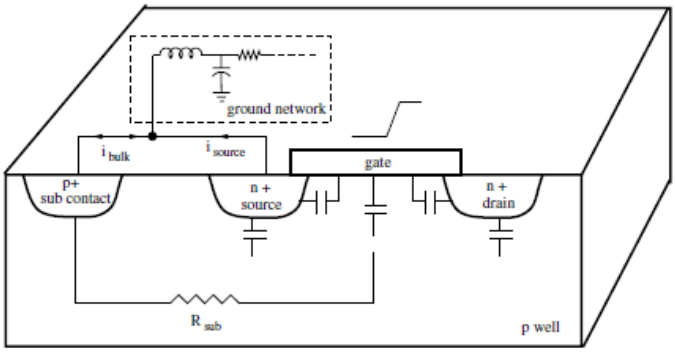


Figure 22 Interaction of chip substrate and ground network

Power ground noise on the package can affect the chip as well when resorting to embedded actives. It is well known that in high-frequency (GHz) packages electromagnetic interference can potentially hamper the normal functioning of the package. In the case of packages with embedded actives, since the chip is housed within the dielectric layers of the substrate, it is prone to the interference from the electromagnetic fields generated in the package. Thus, this interaction needs to be studied to design efficient packages that can support embedded chips. This dissertation focuses on the effects of electromagnetic (EM) interference between the embedded chip and package which include: *1) EM coupling to the chip bond-pads and 2) EM coupling to the chip substrate.*

1.4. Contributions and Outline of Dissertation

Power integrity plays an important role in driving a system's performance. It is essential to acquire an in-depth understanding of the issues that impact the power integrity of packages with embedded actives in order to adopt this emerging packaging technology. As explained before, the predominant challenge in multilayer packages with embedded chips is managing the electromagnetic coupling through the power distribution network. Noise coupling through the power distribution network occurs in multilayer substrates when cavities are formed to embed chips. The sizes of apertures formed to accommodate the embedded chips are much larger than slots and via holes. Hence, the intensity of coupling is higher than what has been analyzed in literature for multilayer packages with vias and slots. Coupling suppression methods available in literature, that target vertical coupling in multilayer packages, are not suitable for providing broadband isolation at high frequencies. A technique for suppressing vertical coupling at high frequencies based on Electromagnetic Band Gap (EBG) structures is a major contribution of this thesis. There are methods in literature that focus on analysis of EBG structures in a single plane pair cavity. In the case of systems with embedded actives, the need is to have a suitable design methodology for EBGs used in multilayer stack-up for vertical coupling suppression. A methodology for synthesizing EBG structures in multilayer packages to provide coupling suppression in desired frequency bands forms the second major contribution of the thesis. The significant novelty in the embedded actives comes from the fact that the package now houses cavities and chips within those cavities. The presence of the chip embedded within the package introduces new interaction mechanisms between the chip and package that have not been encountered in

conventional packages with surface mounted chips. It is of a significant importance to understand the chip-package interaction mechanisms, for ensuring satisfactory design of systems with embedded actives. The final contribution is the analysis of the impact of electromagnetic coupling from the package power/ground layers on the bond pads of the embedded chip and the coupling of the EM fields with the substrate of the embedded chip.

To summarize, the motivation of this dissertation is to address power integrity problems in multilayer packages with chips embedded within the substrate layers and to develop solutions for electromagnetic (EM) interference and noise coupling encountered in these packages. **This dissertation establishes the important factors that impact the noise coupling within the package when cavities are made in the substrate to embed chips, develops a suitable suppression technique to tackle noise coupling, and demonstrates the factors due to which the chip experiences strong electromagnetic interference when embedded within the substrate cavity. Furthermore, the dissertation puts forth a design methodology for suppression of coupling and presents guidelines for designing efficient power distribution networks in multilayer packages with embedded chips.**

The key aspects of the dissertation, which is pictorially shown in Figure 23, are listed below:

1. Identification of the electromagnetic effects in multilayer packages with an embedded chip
2. Analysis of electromagnetic coupling in packages with substrate cavities

3. Analysis of the effect of electromagnetic coupling on the embedded chip and its bond pads
4. Development of a method to counter electromagnetic coupling in multilayer packages with embedded chips
5. Design guidelines for power distribution in packages with embedded chips

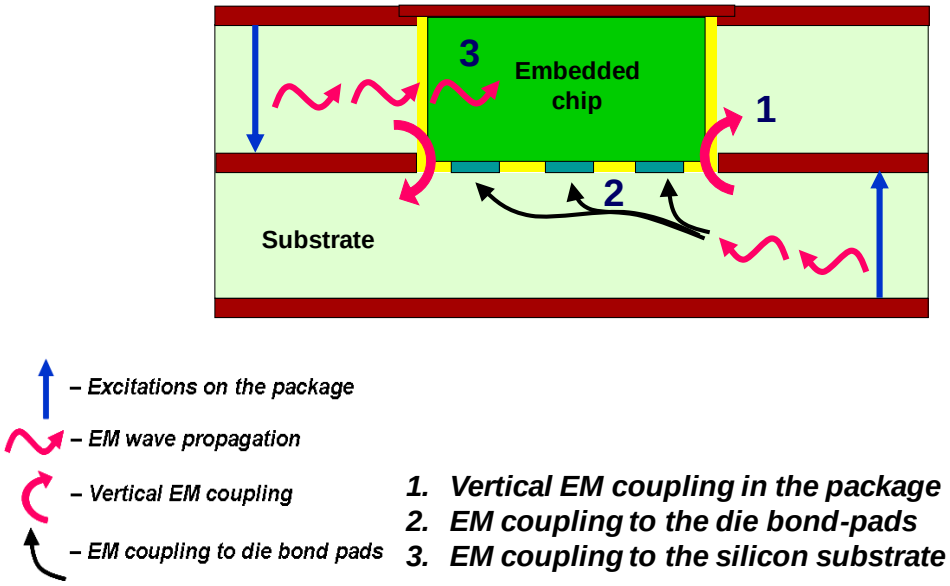


Figure 23 Research topics explored in the dissertation

The dissertation is broadly organized as follows. Chapter 2 describes the effect of cavities in multilayer substrates on the electromagnetic coupling in packages. Chapter 3 proposes a suppression methodology to tackle the horizontal and vertical coupling in packages with embedded ICs that is effective even in the high (GHz) frequency ranges. Chapter 4 discusses an EBG synthesis methodology which is applied to predict vertical coupling suppression. Chapter 5 demonstrates the effects of electromagnetic coupling on the bond pads of the chip embedded within the substrate cavity. Chapter 6 analyses the

effect of coupling on the silicon substrate of the embedded chip when the cavity is closed with a grounded plane. Finally, Chapter 7 presents design guidelines and provides concluding remarks. Now, an outline of the dissertation is provided along with the contributions of each of the chapters.

1.4.1 Vertical Electromagnetic Coupling in Packages with Embedded Chips:

Chapter 2 deals with power/ground noise coupling in multilayer substrates when cavities are formed to embed chips. This chapter analyzes structures with different power/ground stack-up and embedded ICs. Test vehicles are fabricated incorporating different multilayer structures with cavities in the substrate. The simulation results for these structures are validated with frequency domain based VNA measurements. This analysis on coupling phenomenon in substrates with cavities gives insights into the effects of parametric variations, such as cavity sizes, aperture effects on successive metal layers, and presence of the apertures on the noise coupling from one power/ground cavity to another.

1.4.2 Suppression of Vertical Electromagnetic Coupling:

Chapter 3 proposes an effective approach for suppressing vertical electromagnetic coupling in multilayer packages operating at high frequencies. In the case of packages with embedded actives where there are large apertures (die sized) in the metal planes and cavities in dielectric layers to accommodate the chips, the effect of electromagnetic coupling across the package layers is significant. The coupling suppression method involves planar electromagnetic band-gap (EBG) structures for suppressing vertical

coupling. Also, the isolation band over which suppression is achieved can be tuned over different frequency ranges.

1.4.3 : Stop-Band Prediction for Electromagnetic Band Gap Structures in Multilayer Packages

In Chapter 4, a methodology to synthesize EBGs, given the stop band and pass band frequencies as inputs, is developed. A more rigorous methodology for predicting the pass bands and stop bands when the synthesized EBGs are implemented for vertical coupling suppression in multilayer packages is described. These methodologies are demonstrated through simulations and measurements.

1.4.4 Chip-Package Interaction in Packages with Embedded Chips: Electromagnetic Coupling on Chip Bonds

Chapter 5 analyzes the effect of electromagnetic coupling on the bond pads of the embedded chip. In multilayer packages with embedded ICs, the bond pads of the chip experience voltage fluctuations due to noise coupling directly to the bond pads from the power distribution network of the package. Test vehicles with various configurations of power and ground planes are fabricated and the results from simulations and measurements in frequency domain are presented. Time domain simulations are performed to estimate the voltage fluctuation at the bond pads for various noise source locations.

1.4.5 Chip-Package Interaction in Packages with Embedded Chips: Electromagnetic Coupling on Chip Substrate:

In Chapter 6, the effect of covering the cavity enclosing the embedded chip using a grounded plane for grounding the back metallization of the chip or for better heat dissipation is analyzed. This causes the electromagnetic waves from the package power distribution network to couple with the chip substrate. The EM waves injected into the bulk substrate can affect the proper working of the on-chip active and passive circuits. This chapter analyzes the interaction between the chip and the package in terms of the influence the embedded chip has on the EM coupling across the package and the effect of the EM waves coupling to the bulk substrate of the embedded chip.

1.4.6 Conclusions and Future Work:

In Chapter 7, an overview of electromagnetic coupling for multilayer packages with various configurations of power distribution network is presented and the various effects analyzed through chapters 2 to 6 are summarized. Design guidelines for packages with embedded ICs are provided based on the findings in each chapter.

CHAPTER 2

VERTICAL ELECTROMAGNETIC COUPLING IN PACKAGES WITH EMBEDDED CHIPS

The Chip-last method creates cavities in the substrate dielectric material to embed chips. The presence of these cavities causes large die-sized apertures on the power and ground planes of the package. These apertures result in significant levels of noise coupling from one power ground cavity to another. The analysis carried out in this chapter is important to understand the extent of vertical coupling that occurs in packages with cavities and the impact of chips embedded within the cavities on the coupling across the various layers of the package. This chapter discusses the phenomenon of vertical electromagnetic coupling in packages with cavities to house embedded chips.

2.1. Mode of Vertical Coupling in Multilayer Substrates

In multilayer packages, there are multiple power and ground planes which form the power distribution network (PDN). These power and ground planes behave as parallel plate waveguides and exhibit resonances at certain frequencies depending on the geometry of the planes and the dielectric materials used in the package. When vias, which are the vertical interconnects penetrate a plane pair formed by a combination of a power and ground plane, a current source is setup due to the accumulation of opposite charges on the power and ground planes thereby generating electromagnetic (EM) waves. The EM waves excite the cavity resonances causing unwanted interference with victim circuits that are powered by the same power and ground plane pair. When multiple fast

switching drivers switch simultaneously exciting the cavity, the unwanted interference is more severe and appears as large voltage fluctuation in the plane pair cavity. This noise is called simultaneous switching noise (SSN). The noise generated in the form of voltage fluctuation gets transmitted horizontally across the power-ground cavity by electromagnetic wave propagation. When there are apertures in the planes, SSN couples vertically across multiple plane pair cavities as well. SSN is detrimental to the power integrity of the system as the voltage fluctuations that are induced in the system can cause logic errors and false switching of circuits.

The presence of apertures in the power and ground planes of multilayer packages causes electromagnetic (EM) waves to fringe through the aperture from one plane pair cavity to another resulting in field coupling. This is shown in Figure 24 and Figure 25 with the help of wrap-around currents and electromagnetic wave propagation. Figure 24 shows a three metal layer structure with an aperture in the middle plane, which is labeled as M2. The excitation with a current source in plane pair cavity 2 (referenced between M2–M3 layers) causes the flow of surface currents on the bottom side of M2. When these currents encounter the aperture, they wrap around and flow in the top cavity. The inherent property of current is that when there is flow of current in a metal conductor in one direction, a return current will flow in opposite direction in another conductor that is in close proximity to the current carrying metal conductor. Due to this effect, there is a flow of return current on the bottom side of M1. The forward and reverse currents in M2 cause electromagnetic wave propagation in the top plane pair cavity as shown in Figure 25. Thus, the field produced in the bottom plane pair cavity, couples to the top plane pair cavity without the top cavity being excited. Note that Figure 24 and Figure 25 show

related phenomena of wrap-around currents and the resulting wave propagation. They are shown separately for ease of understanding the effects.

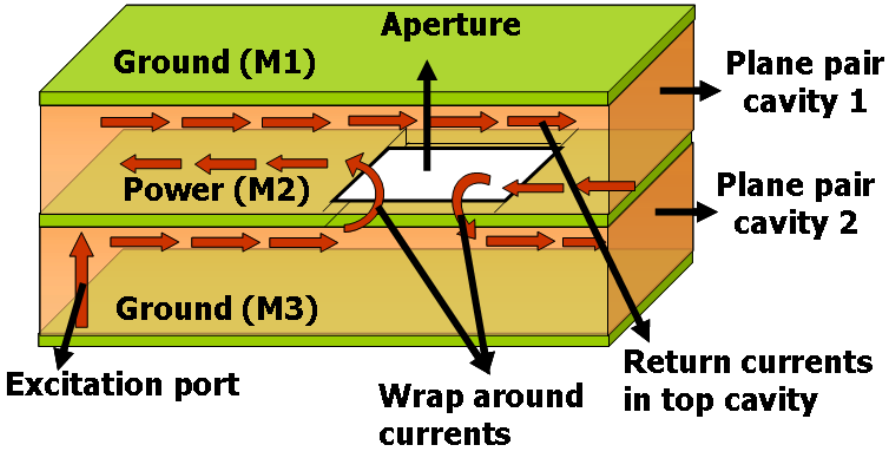


Figure 24 Vertical coupling through apertures - wrap around current

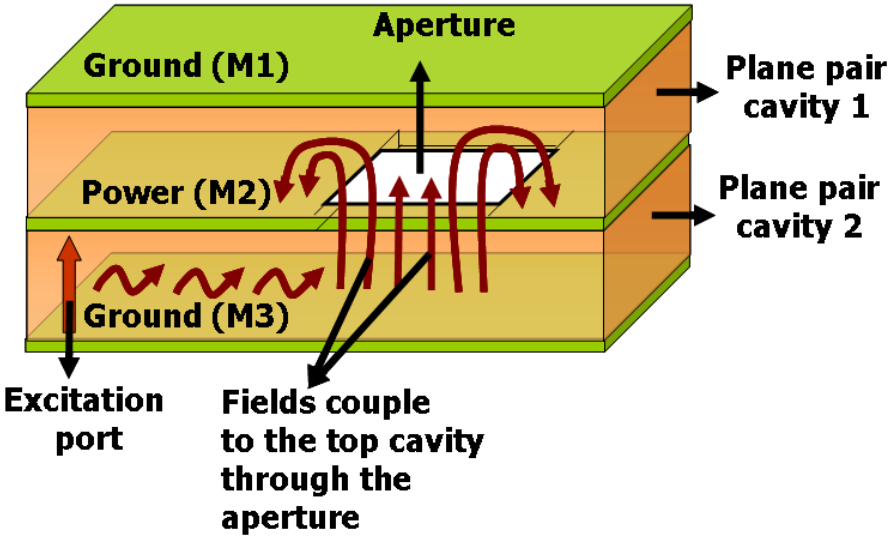


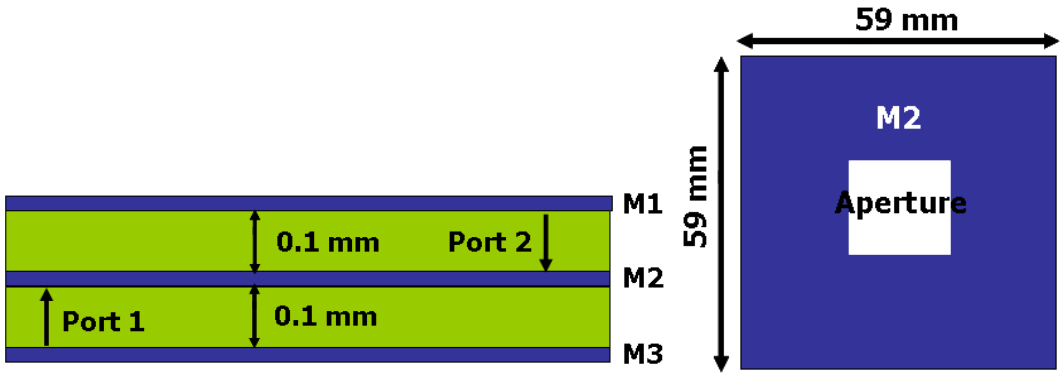
Figure 25 Vertical coupling through apertures - Electromagnetic wave propagation

2.2. Parametric Variations Influencing the Coupling between Power-Ground Plane Cavities

To demonstrate the effect of aperture size on vertical coupling in multilayer packages, a three metal layer structure, with lateral dimensions of 59 mm X 59 mm and

excitation (Port 1) and response (Port 2) port locations as shown in Figure 26a is simulated. Figure 26b shows the top view of M2 layer which has the aperture. The ports represent current source locations, which are used to excite the plane pair cavity. In this section, simulations are performed with apertures of different sizes to investigate the SSN coupling across multiple plane pair cavities.

For simulation purposes, the size of the aperture is varied as — 10 X 10 mm, 4 X 4 mm, 2 X 2 mm, 1 X 1 mm and 0.5 X 0.5 mm. In the stack up shown in Figure 26a, plane M1 and M3 are used as grounds and M2 is used as power (Vdd). Port 1 is referenced between M2–M3 metal layers while Port 2 is referenced between M1–M2 metal layers. The graph, shown in Figure 27, shows the coupling for different sized apertures in terms of S-parameters measured across the two ports (S21 (dB)). As seen from the graph, as the aperture size decreases, the coupling occurring through it reduces. Based on this, for apertures of size 0.5 X 0.5 mm, the coupling that occurs across the two plane pair cavities, which is about -50 dB, is not significant. Note that the coupling will be lesser than -50 dB for apertures of even smaller sizes. In Figure 28, the result from coupling through a slot is shown. For long slots or split planes and for apertures greater than 1 X 1 mm required by some embedded chips, the vertical coupling will be significant as seen from Figure 27 and Figure 28. This analysis demonstrates that the vertical coupling encountered in the case of packages with apertures to embed chips is higher as compared to that caused by anti via holes and connector holes.



a) b)

Figure 26 a) Cross-section of the three-metal layer structure, b) Top view of M2 layer with aperture

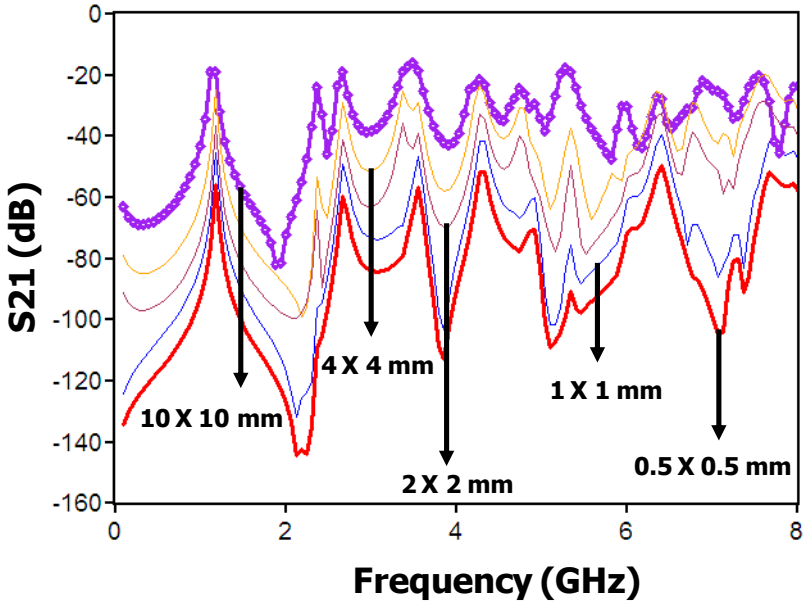


Figure 27 S21 (dB) results for different sized apertures in the structure shown in Figure 26

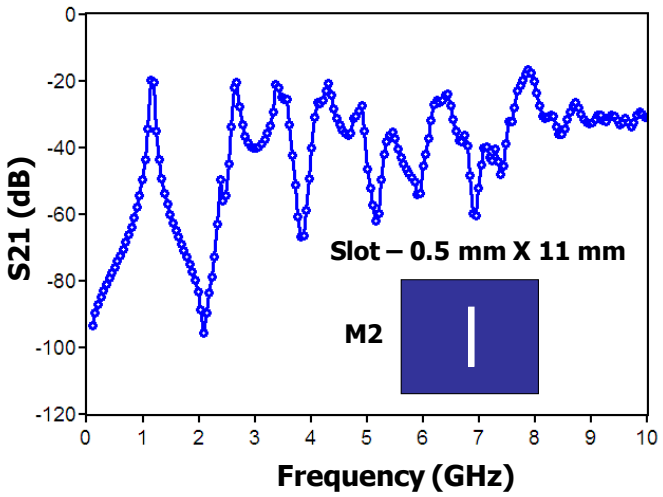


Figure 28 S21 (dB) results for a slot in the structure shown in Figure 26

2.3. Design and Modeling of Structures with Dielectric Cavities and Apertures in Metal Planes

The analysis performed above focused on the size of apertures. In this section, two other variations are studied, which takes the analysis closer to the real case of embedding a chip within a package. As shown in Figure 9 (Chapter 1), the embedded chip in some configurations can also extend across multiple metal layers. In such a case apertures need to be formed on successive metal layers as well as requiring a dielectric cavity to accommodate the chip. In this section, an analysis is performed to show the effect of having apertures on successive metal layers, the effect of forming dielectric cavities and that of the clearance between the embedded chip and the surrounding dielectric cavity. Figure 29, Figure 30 and Figure 31 show the three different configurations analyzed in the simulations. In these figures, S1 refers to Figure 29, S2 to Figure 30, and S3 to Figure 31. The stack-up details are shown in Figure 32, while Figure 33 shows the position of the aperture.

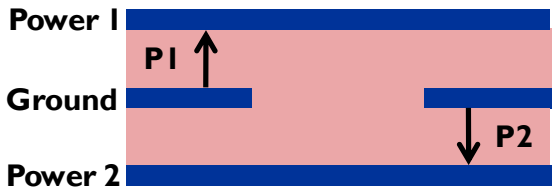


Figure 29 Structure 1 (S1)

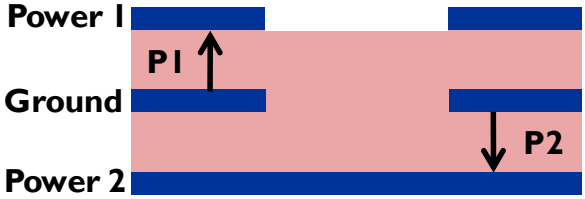


Figure 30 Structure 2 (S2)

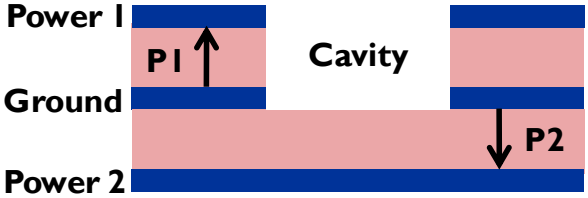


Figure 31 Structure 3 (S3)

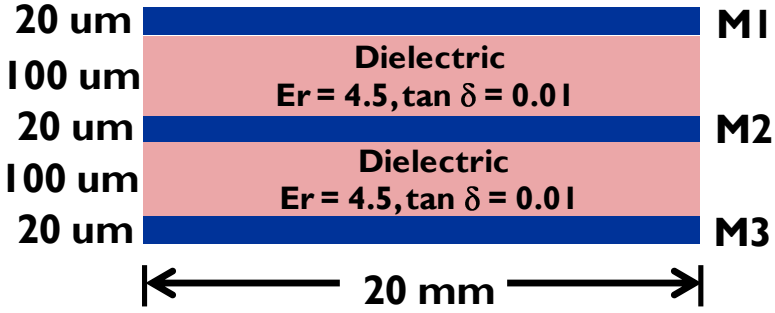


Figure 32 Three metal layer stack-up where M1, M2 and M3 layers are provided power/ground assignments as shown in Figure 29, Figure 30, and Figure 31

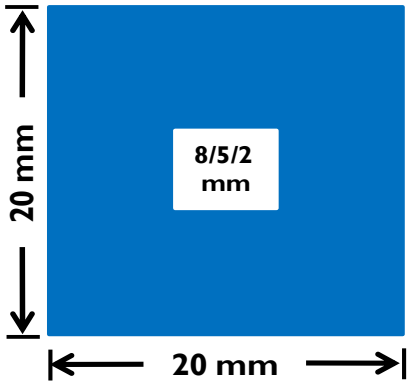


Figure 33 Top view showing the location aperture in M1 and M2 layers of Figure 32

In all these structures port 2, P2 (between M2 and M3 layers) is excited and the S-parameter S21 is plotted in dB scale to observe the noise that is getting coupled to the un-excited port 1, P1 (between M1 and M2 layers). In the ideal case, when the planes are fully continuous, the S21 values should be low (negative values) indicating almost zero coupling. But the presence of apertures in the planes causes the electric field to couple from one power-ground cavity to another. The frequencies at which a plane pair cavity experience resonances is calculated using the formula,

$$f_{mn} = \frac{c}{(2 \times \pi \times \sqrt{\varepsilon_r})} \times \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2}$$

where c – velocity of light (3 X 10^8 m/s)

f_{mn} – resonant frequency for the mode (m,n) in Hz

ε_r – dielectric constant of the material in the parallel plate cavity

a, b – lateral dimensions of the planes (for the simulations here, they are equal) in m

m, n – propagating modes in the parallel plate cavity

For the planes considered here, the (1, 0) and (0, 1) modes occur at 3.53 GHz, (1, 1) mode occurs at 5.0 GHz, mode (2, 0) occurs at 7.07 GHz, and modes (2, 1) and (1, 2) occur at 7.91 GHz. Figure 34 shows the results from Structure 1 for vertical coupling between ports P1 and P2 for three different aperture sizes (2 X 2 mm, 5 X 5 mm and 8 X 8 mm). From Figure 34 it is observed that the coupling between adjacent power/ground cavities is significant not only at these resonant frequencies of the parallel plate cavity but also at certain other frequencies where the aperture resonances occur, such as 2.6, 2.95, 5.8 and 7.45 GHz. Figure 35, Figure 36 and Figure 37show the results for S1, S2 and S3 with aperture sizes of 2 mm, 5 mm and 8 mm respectively. The fields that fringe from the edges of the aperture as shown in Figure 38 result in vertical coupling [**57**]. The frequencies at which the coupling due to the fringing fields is significant are dependent on the size of the aperture. As the aperture size increases, the resonances caused by the fringe fields from the apertures, move away from the parallel plate mode resonances. This effect is observed in Figure 35, Figure 36 and Figure 37. Due to the presence of apertures on successive metal layers, the parallel plate modes are suppressed and the resonances observed in the vertical coupling are caused by the apertures. The change in the dielectric material within the cavity does not affect the frequencies at which the resonances are caused by the fringe fields in the vertical coupling across the plane pair cavities, Power1 – Ground and Power2 – Ground. Due to this, the resonances in the vertical coupling in Structure 3 remain similar to the result from Structure 2 (shown in Figure 35).

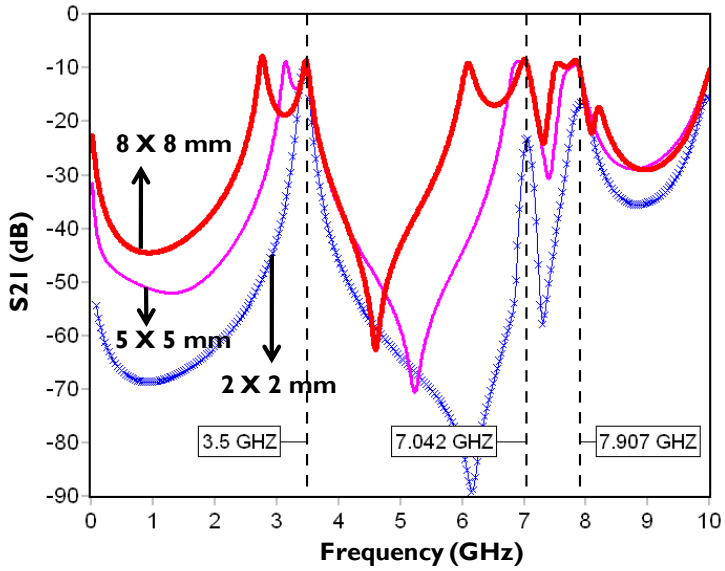


Figure 34 S21 in dB for S1 corresponding to aperture sizes of 2 X 2 mm, 5 X 5mm and 8 X 8 mm

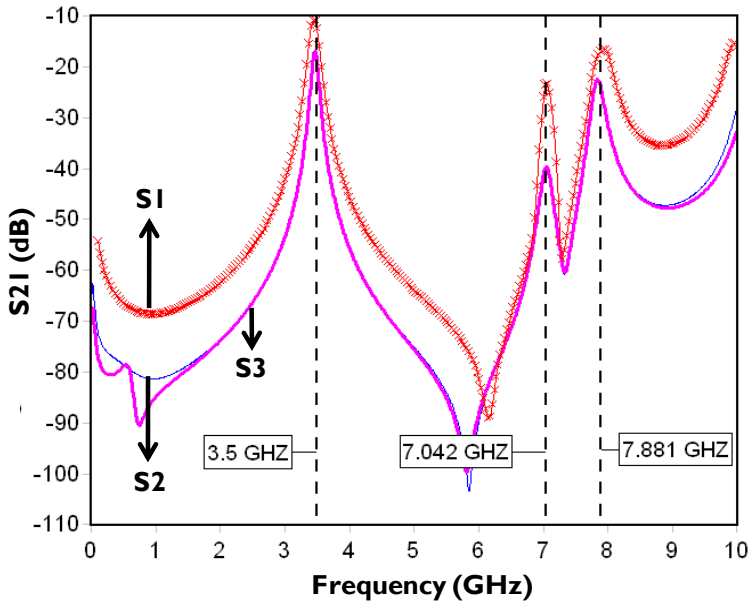


Figure 35 S21 in dB for structures S1, S2, and S3 and aperture size of 2 X 2 mm

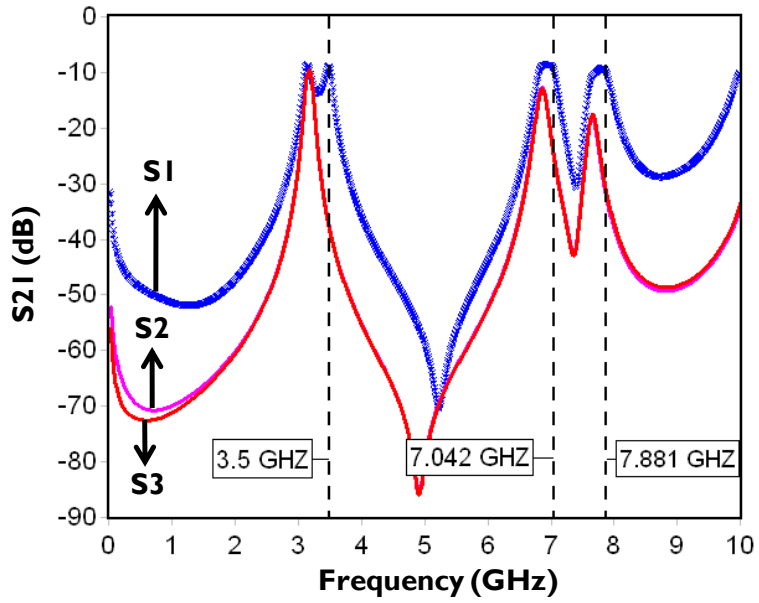


Figure 36 S21 in dB for structures S1, S2, and S3 and aperture size of 5 X 5 mm

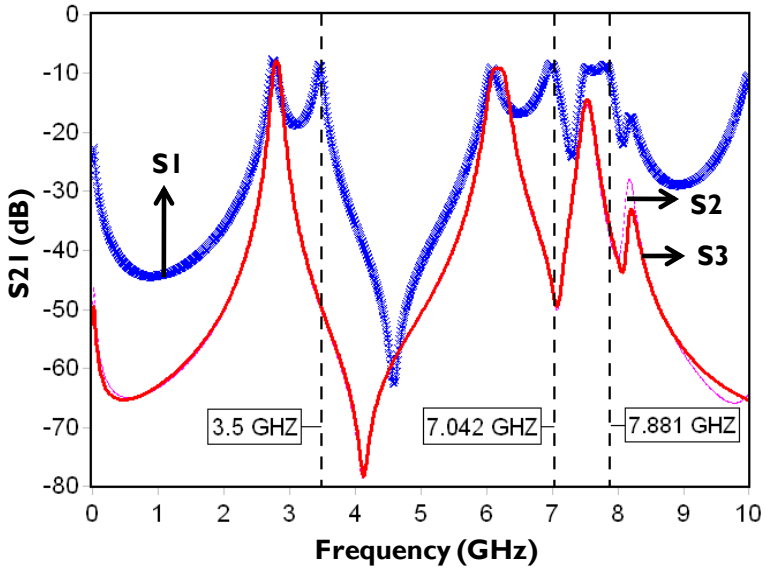


Figure 37 S21 in dB for structures S1, S2, and S3 and aperture size of 8 X 8 mm

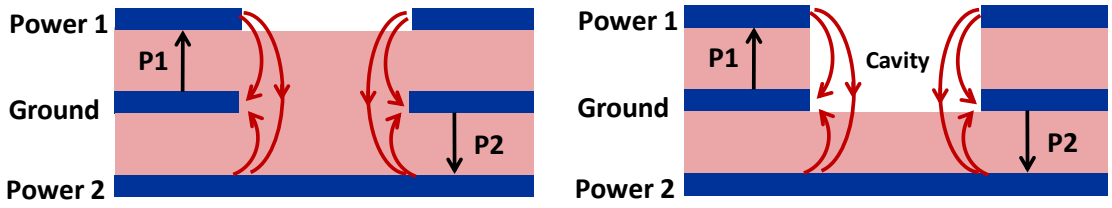


Figure 38 Structures S2 (Left) and S3 (Right) with fringe fields marked with curved arrows across the plane pair cavities

Next, the effect of the die to cavity clearance for embedded silicon chips of conductivities 10 S/m and 20 S/m are analyzed. These values are chosen to represent regular CMOS grade conductivities and high resistivity grade silicon. In Figure 39, a cross-section of a three metal layer structure with the embedded chip is shown. In the plots showing the results, this structure is referred to as S4. In the simulations here, clearances of 50 um and 25 um on each side between the die and cavity are analyzed. The stack-up used is same as in Figure 32 except that the thickness of each dielectric layer is 300um for the simulations in Figure 40 and Figure 41and it is 25 um for the simulations in Figure 42. The die to cavity clearance that has been achieved so far in fabrication is 100 um [**55**]. This is discussed in the next section where measurement results are presented. In Figure 40 and Figure 41 the results from S4 for conductivities of 10 S/m and 20 S/m are compared with the results from structures S2 and S3 for the cavity clearances of 50 um and 25 um respectively. In Figure 42, the results from S4, S3 and S2 are shown for a dielectric layer thickness of 25 um and die to cavity clearance of 25 um. From these figures it can be seen that the effect of embedding the silicon does not influence the fringe field coupling across multiple plane pair cavities down to a die-cavity clearance of 25 um.

This result is significant as it can be used to make the modeling of embedded actives simpler. Especially, modeling the under-fill profile within the cavity as shown in Figure 39 is very difficult. If one were to estimate the frequencies at which the vertical coupling caused by the fringe fields are significant, a simpler model with a homogeneous dielectric but with appropriate apertures in the metal layers can be used. The effect of the dielectric material on the fringe field is not significant to shift the location of the frequencies at which resonances are caused by the fringe fields. So, a simpler model is a good enough approximation.

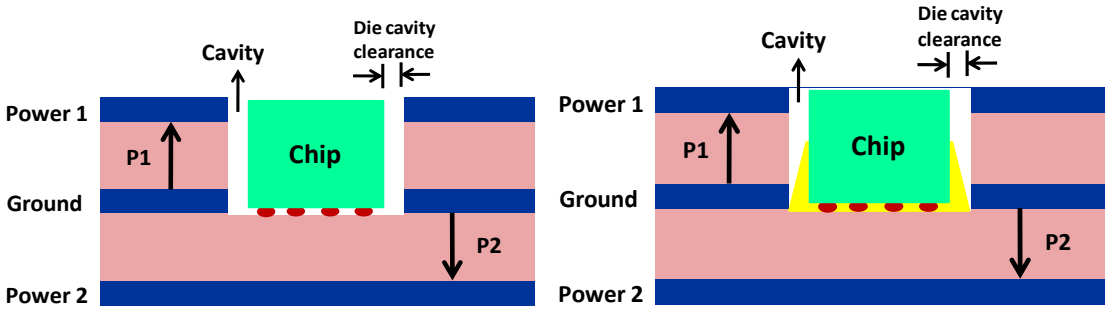


Figure 39 Structure 4 (S4) showing the cross-section with embedded chip. There is no under-fill in the figure on the left and the figure on the right shows the profile of under-fill material inside the cavity

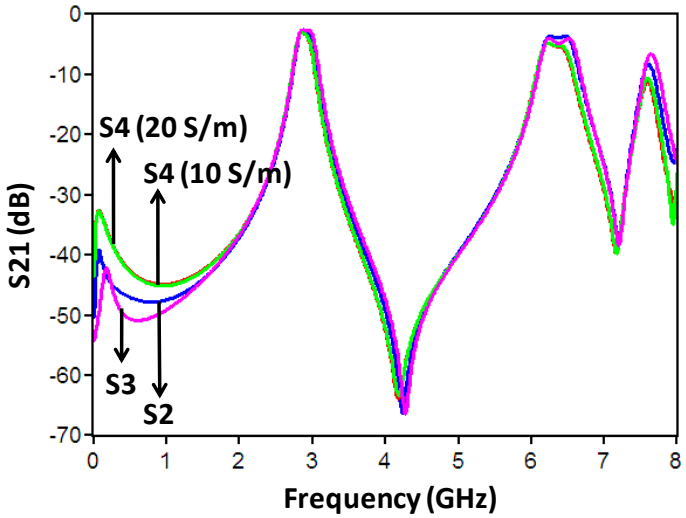


Figure 40 S21 in dB for S2 and S3 with an aperture of 8 X 8 mm and die to cavity clearance of 50 um for conductivity 10 S/m and 20 S/m.

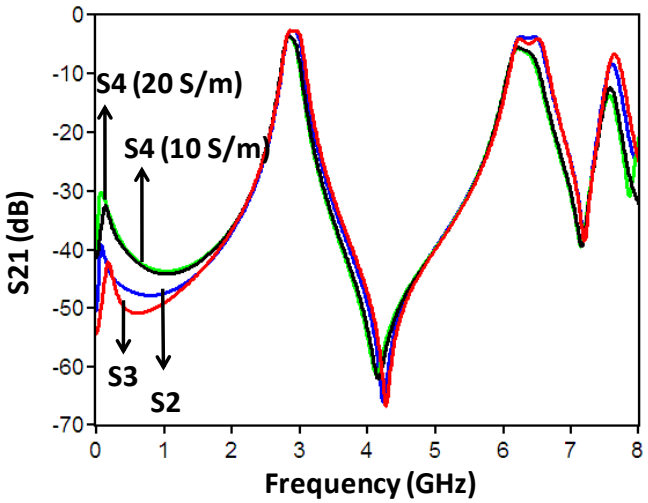


Figure 41 S21 in dB for S2 and S3 with an aperture of 8 X 8 mm and die to cavity clearance of 25 um for conductivity 10 S/m and 20 S/m.

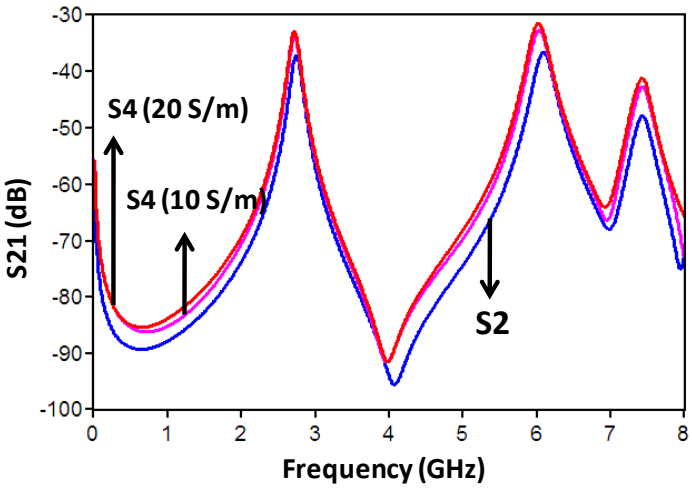


Figure 42 S21 in dB for S2 and S3 with an aperture of 8 X 8 mm, dielectric thickness of 25 um and die to cavity clearance of 25 um for conductivity 10 S/m and 20 S/m.

2.4. Fabrication of Test Vehicle for Power/Ground Plane Stack-up

A test vehicle consisting of three metal layers (M1, M2 and M3) and two build-up dielectric layers is fabricated to demonstrate the vertical coupling described in Section 2.1. Figure 43 shows a schematic representation of the cross-section of the test vehicle along with the top view of the plane with aperture. Photo-imageable dielectric (PID) Probelec-81/7081 (Huntsmann–Vantico Inc.) is used for making the dielectric build-up layers. For substrate core, copper-clad BT (Bismaleimide Triazine) of 500 um in thickness is used. The thickness of each of the dielectric layers is 50 um (with a tolerance of +/- 5 um) and the metal layers are 10 um thick. Photo-cavity process is used to make cavities in the dielectric material. The primary concern during the fabrication processes was the shorting of adjacent metal planes through the cavity opening during electrolytic plating. The photoresist that covers the electroless copper plated seed layer tends to bend at the cavity edge forming crinkles at the bends causing the electroplating copper to seep

through. If this happens, it will short adjacent metal planes. So a stepped cavity structure is adopted for Structures 3, which involves cavities in dielectric layers. Note that such a precaution is not required in Structures 1 and 2 as they do not have any dielectric cavities. As shown in the Figure 44, a 100 um clearance is provided on each side of the cavity to avoid the copper from reaching the next layer. Figure 45 shows the layout of the test vehicle consisting of 12 coupons, 4 each for Structures 1, 2 and 3.

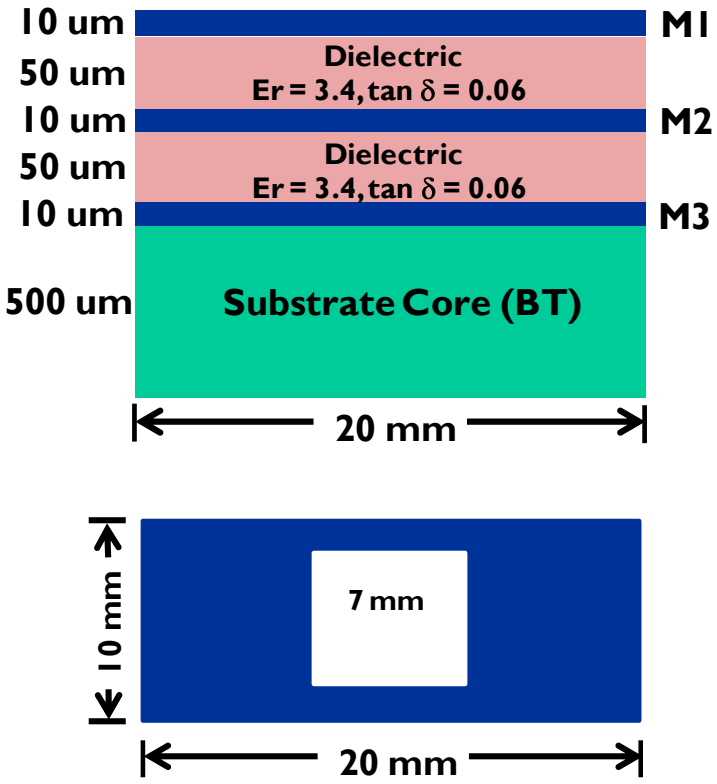


Figure 43 Power/Ground Plane stack-up used for fabrication

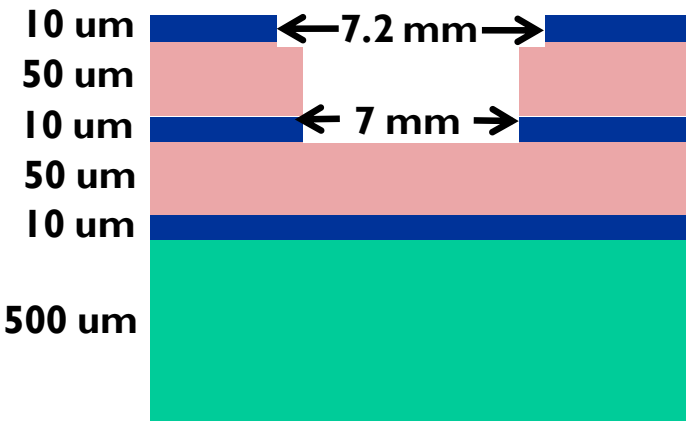


Figure 44 Stepped Cavity structure

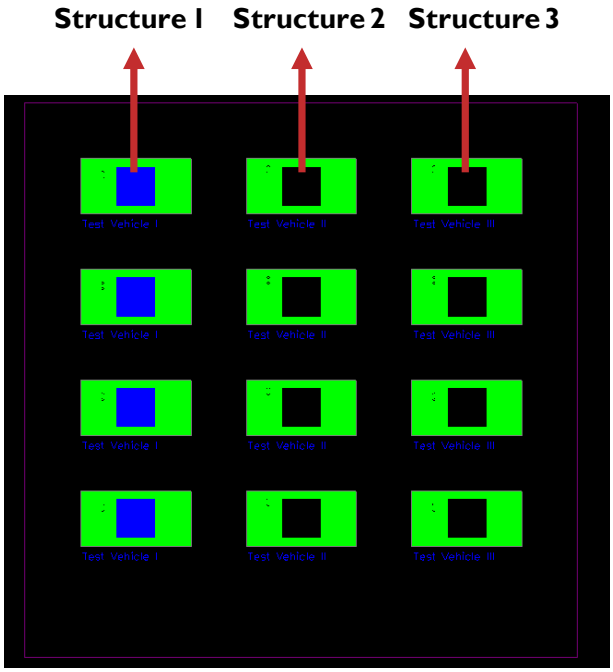


Figure 45 Test vehicle layout with three different structures for Power/Ground stack-up

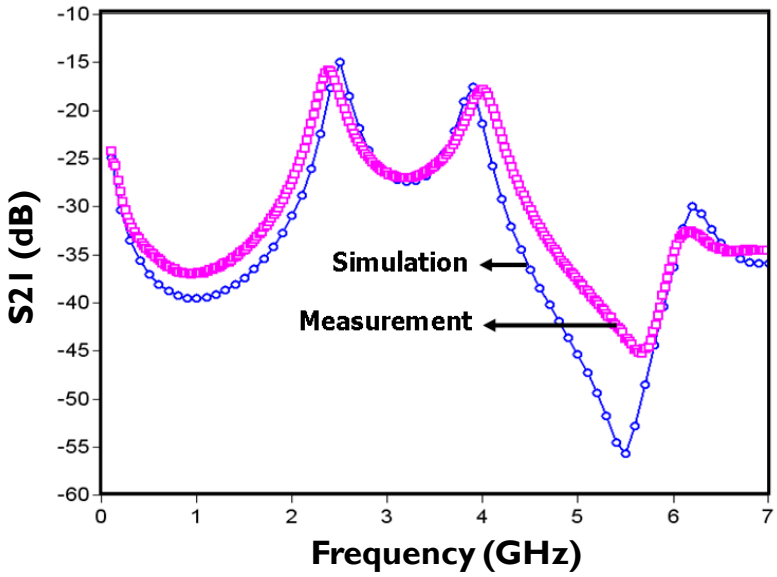


Figure 46 Comparison of simulation and measurement results for Structure 1

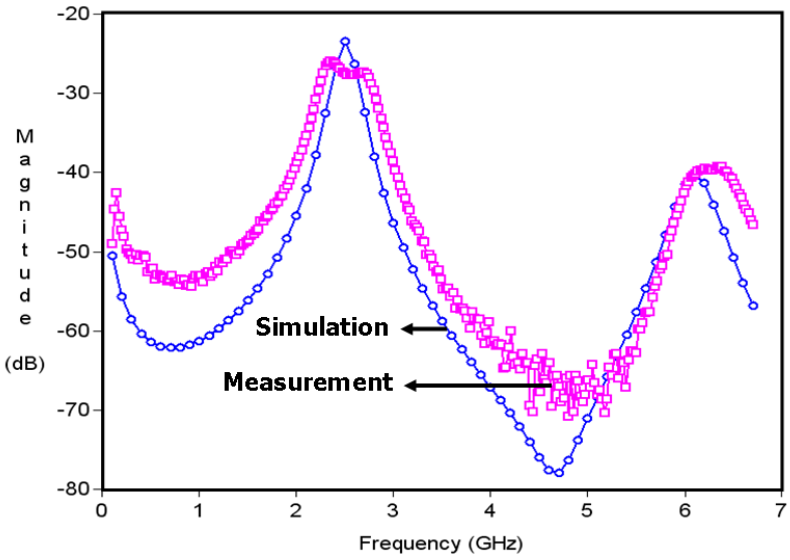


Figure 47 Comparison of simulation and measurement results for Structure 2

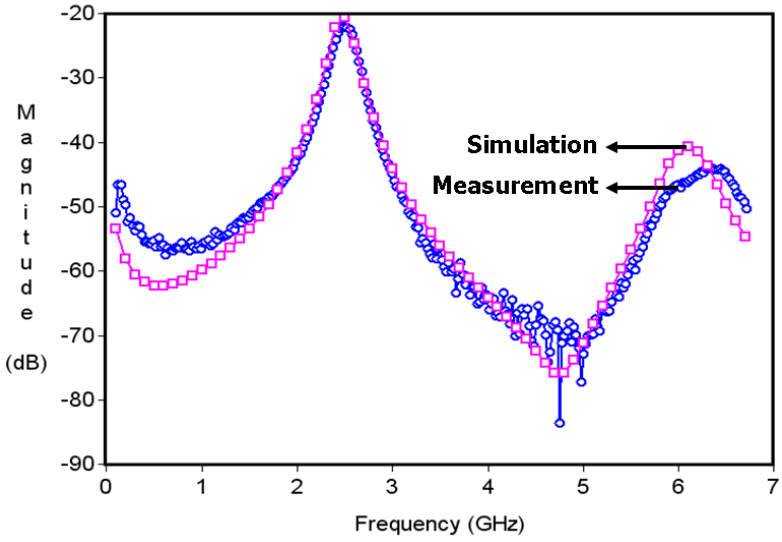


Figure 48 Comparison of simulation and measurement results for Structure 3

The S-parameter measurements are carried out using a vector network analyzer (VNA) and air coplanar probes of pitch 500 um. The measurement and simulation results in Figure 46, Figure 47 and Figure 48 show good agreement. The simulations were performed using the EM solver Ansoft HFSS. The variations observed between the measurement and simulation results below the level of -50 dB are not considerable enough to account. The results indicate the significance of vertical coupling in packages with embedded chips and also the frequencies at which resonances occur due to fringe fields in structures 2 and 3 coincide.

2.5. Concluding Remarks

To summarize, Chapter 2 dealt with power/ground noise coupling in multilayer substrates when cavities are formed to embed chips. This chapter analyzed different power/ground stack-up structures with chip-last embedded actives. Test vehicles were fabricated incorporating different multilayer structures with dielectric cavities. The

simulation results for these structures were validated with VNA measurements in frequency domain. This analysis on coupling phenomenon in substrates with cavities gave insights into the effects of parametric variations, such as cavity sizes, apertures on successive metal layers, and presence of dielectric cavities on the noise coupling from one power/ground cavity to another. Following are the major findings of the chapter:

1. Apertures that accommodate embedded chips result in significantly higher vertical coupling as compared to apertures for vias and connectors.
2. When apertures are formed on successive metal layers, the resonances in the vertical coupling across multiple plane pair cavities is significant corresponding to the resonances caused by fields fringing from the apertures.
3. The removal of the dielectric material to form the cavity to embed the chip does not significantly influence the vertical coupling in the package.
4. The die to cavity clearance does not influence the vertical coupling down to a clearance of 25 um. This result is significant in the sense that it would make modeling of packages with embedded actives simpler.
5. Test vehicles were fabricated incorporating different multilayer structures with dielectric cavities. The measurement results agreed well with the simulation results.

CHAPTER 3

SUPPRESSION OF VERTICAL ELECTROMAGNETIC COUPLING

Electromagnetic coupling is detrimental to the efficient operation of power distribution network (PDN) in a package. Owing to reduction in package sizes, the resonances caused by power/ground planes of the PDN occur in the GHz frequency range. Electromagnetic coupling across the PDN is strongest at the resonant frequencies and causes peaks in the transfer impedance profile across various locations in the multiple layers of the PDN. As explained in Chapter 2, the vertical coupling caused by fringe fields from the edges of large (die sized) apertures in metal planes and cavities in dielectric layers was found to be significant in packages with embedded chips. The intensity of the coupling encountered and the frequencies at which it is predominant make it necessary to explore new methods to effectively mitigate the noise across the system when resorting to embedding chips. In this chapter, an effective approach for suppressing vertical electromagnetic coupling in multilayer packages operating at GHz frequencies is introduced. The method discussed in this chapter, involves planar electromagnetic band gap (EBG) structures for suppressing vertical coupling. The isolation band over which suppression can be achieved is tunable over different frequency ranges.

3.1. Electromagnetic Band gap Structures

Electromagnetic Band Gap (EBG) structures have been widely used for the suppression of electromagnetic wave propagation and radiation. EBGs are periodic

structures consisting of repeated set of patterns that are formed either by drilling the dielectric material of the substrate, or patterning the metallization layers [**79**] [**80**][**81**]. They disrupt the propagation of EM waves due to their periodic discontinuity. EBGs allow the propagation of EM waves in certain frequency bands and reject wave propagation in certain other frequency bands. In other words, they provide pass bands in some frequencies and stop bands in other frequencies. Owing to this property, EBG structures have found applications in antennas [**82**], filters [**83**] [**84**], wave guides [**85**] and other microwave components such as power dividers/combiners, amplifiers [**86**] and phased arrays to name a few [**87**]. The wide stop bands that EBGs offer can be used for providing noise isolation in mixed signal packages. Several configurations of EBGs targeting these various applications have been proposed in literature [**88**] [**89**] [**90**]. In particular, planar EBGs have gained wide usage for noise suppression in mixed signal systems due to their simple design and ease of fabrication [**88**] [**91**]. Planar EBGs used for the purposes of noise isolation in power distribution networks of mixed signal systems work on the principle that when one of the planes in a plane pair cavity is patterned (i.e., with the EBG structure), the propagation of electromagnetic waves between the two planes forming the plane pair cavity is suppressed within a certain frequency band. Alternating Impedance EBG (AI-EBG) [**92**] is a planar EBG that offers high isolation levels in the frequency band for which it is designed. AI-EBG consists of a unit cell that is repeated throughout the power or ground planes, or more generally, whichever plane is chosen to be the EBG plane [**92**]. Figure 49 shows an EBG plane consisting of AI-EBG units cells composed of alternating patches and branches, which offer impedance discontinuity to the propagation of EM waves, thereby providing noise

isolation. Ports 1 and 2 in Figure 49 form the excitation and response points for the AI-EBG structure. When Port 1 is excited, the EM coupling at Port 2 is significantly reduced in the frequency range where the AI-EBG is designed to offer a stop band.

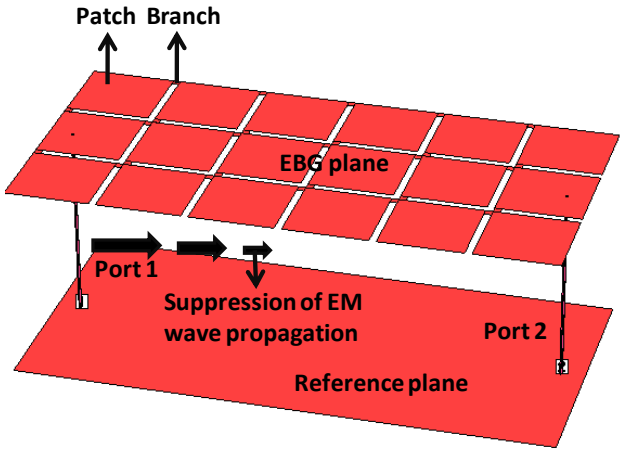


Figure 49 EBG plane patterned with AI-EBG structures

In this chapter, a method for suppressing vertical electromagnetic coupling across multiple plane pair cavities is proposed. This is suitable for mitigating the noise coupling issue when cavities are formed in the packages for embedding chips. This method uses planar electromagnetic band gap structures to achieve the suppression of vertical electromagnetic coupling. Thus far, prior works [**93**] [**94**] [**95**] [**63**] [**96**] [**97**] on EBG structures have addressed coupling suppression only within a single plane pair cavity. The work discussed below is the first demonstration of EBGs for suppression of vertical electromagnetic coupling in multilayer packages.

3.2. Suppression of Vertical Coupling

3.2.1 Coupling suppression in adjacent plane pair cavities

To counteract the vertical coupling shown in Figure 24 (Chapter 2), the middle plane, which has an aperture in the multilayer structure, is patterned to form EBG structures, as shown in Figure 50. The EBGs suppress the propagation of surface currents thus causing a reduction in wrap-around currents at the apertures. This suppresses the propagation of fields through the aperture in the vertical direction and provides considerable isolation between the top and the bottom plane pair cavities [**98**]. It is important to connect the planes above and below the EBGs (M1 and M3 layers) by vias as shown in Figure 52. When the EBG plane is excited, the apertures in the EBG patterns themselves will cause wrap around currents as shown in Figure 51. Furthermore, if there is an isolated plane on top of the EBG plane (i.e., M1), the two planes sandwiching the EBG layer (i.e., M1 and M3) will start supporting forward and return (i.e., in opposite direction to forward) currents. The flow of forward and return currents in the planes forming a plane pair cavity sets up electromagnetic wave propagation within the cavity. Thus the EBG band gap property will be lost if the polarity of the planes on either side of the EBG plane are not maintained the same [**99**]. Hence, M1 and M3 are connected using vias so that they are maintained at the same polarity, thus causing the return currents in M1 to get shorted to M3. The best location to place vias is around the excitation and response ports to achieve a high level of isolation. Now, that M1 and M3 are maintained at the same polarity, the EBG effectively produces a band gap.

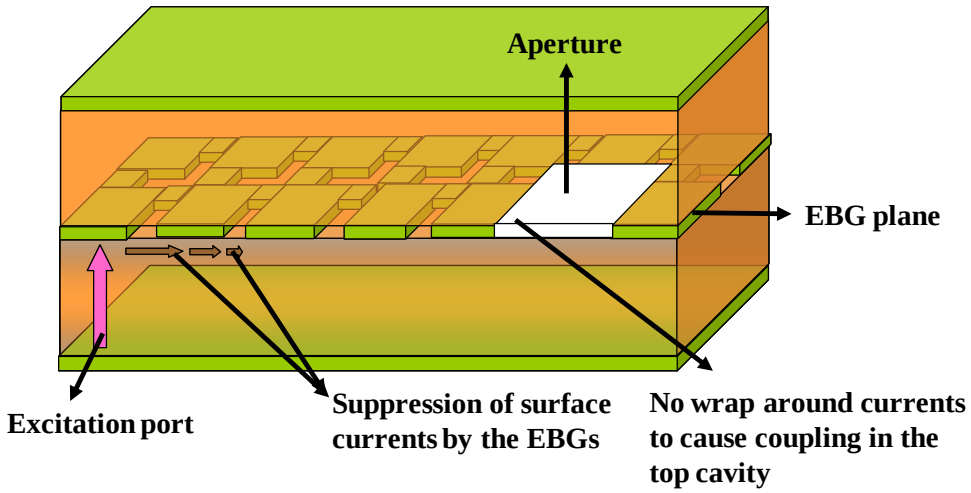


Figure 50 Aperture plane patterned with EBGs

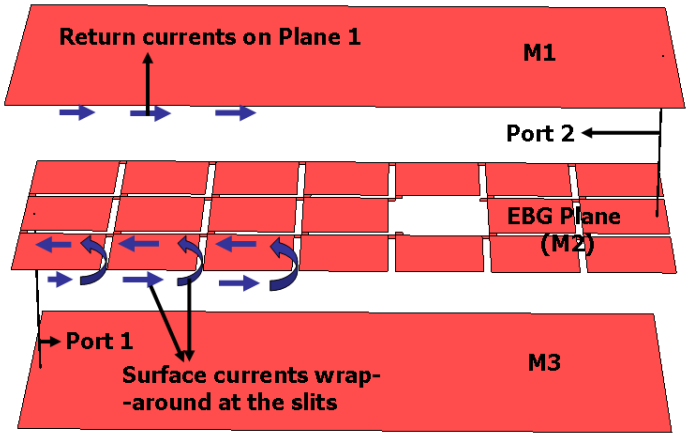


Figure 51 EBG plane sandwiched between two isolated planes

The efficacy of the EBG structures is shown below using a simulation example. All simulations performed in this chapter are using a tool based on Multilayer Finite Difference Method (MFDM) [**64**]. Figure 53 shows the cross-section of the layer stack-up used for the simulation results in this section. The dielectric material used in the stack-up is FR-4 with a dielectric constant of 4.5 and loss tangent of 0.01. Figure 52 shows the multilayer structure with EBGs. This structure uses the first three layers (M1–M3) of the layer stack-up. Port 1 is defined between M2 (EBG plane) and M3, while Port 2 is

defined between M1 and M2. The vias connecting M1 and M3 do not short the EBG plane. The EBG patch size is chosen as 8 mm X 8 mm and the branch size is 0.5 mm X 0.5 mm for this simulation. Figure 54 shows the graphs for the S-parameter responses showing the field coupling between Ports 1 and 2 for the scenarios with and without EBGs. The setup for the no-EBG case is similar to the structure shown in Figure 52, except that there are no EBG patterns on M2 layer and it is solid except for the aperture. As can be seen from Figure 54, high isolation is obtained between the top and bottom plane pair cavities when EBGs are used. Note that the band gap frequency of the EBGs can be tuned by changing the size of the patch and branch, which is the basis for EBG synthesis methodology which would be discussed in Chapter 4.

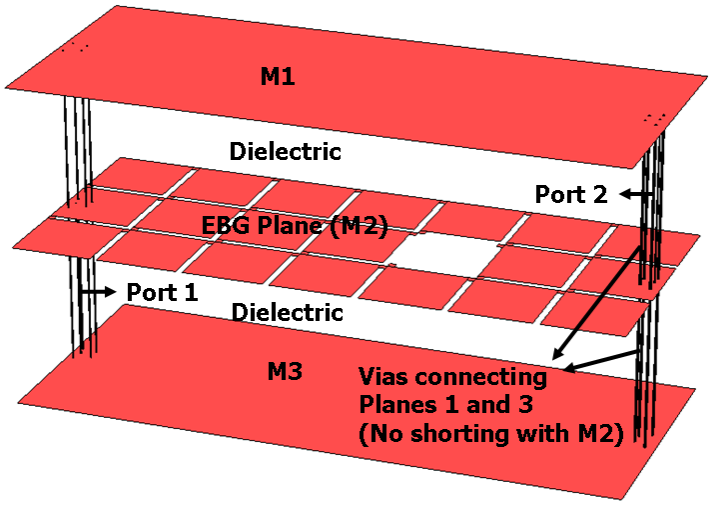


Figure 52 Multilayer structure with EBGs

Figure 53 Substrate layer stack-up used for simulations

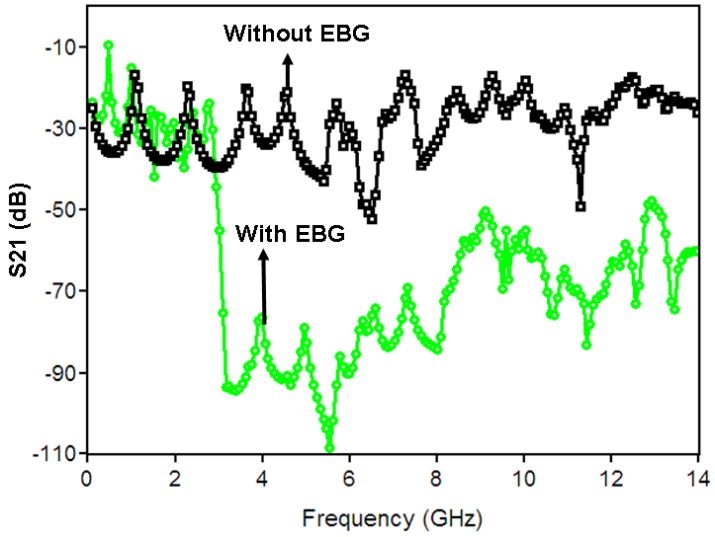


Figure 54 Comparison of isolation with and without EBGs

3.2.2 Coupling suppression in non-adjacent plane pair cavities

In the previous section, EBG structures were shown to provide vertical isolation between two plane pair cavities there were adjacent to each other. Now, this concept is extended to provide vertical isolation in plane pair cavities that are not adjacent to the patterned AI-EBG plane. Figure 55 shows a four layer metal structure with the apertures, ports on the different planes. The structure uses all the four layers of the substrate stack-up (M1–M4). The excitation between M3–M4 (Port 1) results in surface currents in planes M3 and M4. The surface currents on the bottom surface of M3 wrap-around at the

aperture in M3, and due to which forward and reverse currents are induced in M2 and M3 layers, respectively. Again, surface currents on M2 wrap-around at the aperture in M2, which in turn sets up surface currents in the parallel plate cavity formed by M1–M2 pair. Notice how the apertures in M2 and M3 cause coupling across different plane pair cavities. Figure 56 shows the structure with EBGs in which the layers M2 and M4 are shorted with vias. The EBGs suppress the flow of surface currents on both sides of the patterned plane. This in turn suppresses return currents on the bottom side of M2 and reduces wrap around currents through the aperture in M2. So, the flow of currents in the plane pair cavity formed by M1 and M2 is suppressed. Thus, this offers isolation across plane pair cavities 1, 2 and 3. The S-parameter plot in Figure 57 compares the results for the cases with and without EBGs. As shown in the figure, good isolation levels are obtained.

Thus, by appropriately patterning a single layer with EBGs in a multilayer stack-up, it is possible to suppress vertical coupling across multiple layers of plane pair cavities on either side of the patterned plane. This method of suppressing vertical coupling is useful, especially in the case of multilayer packages where coupling needs to be suppressed across multiple plane pair cavities. Of course, this method obviates the need to pattern multiple power planes with EBGs. The magnitude of isolation obtained decreases as we go away from the EBG plane, but the EBG plane can be appropriately placed according to the needs of the application and the isolation levels required for different on-chip aggressors. The simulation examples presented demonstrate how isolation across multiple layers can be achieved while keeping the number of patterned planes to a minimum.

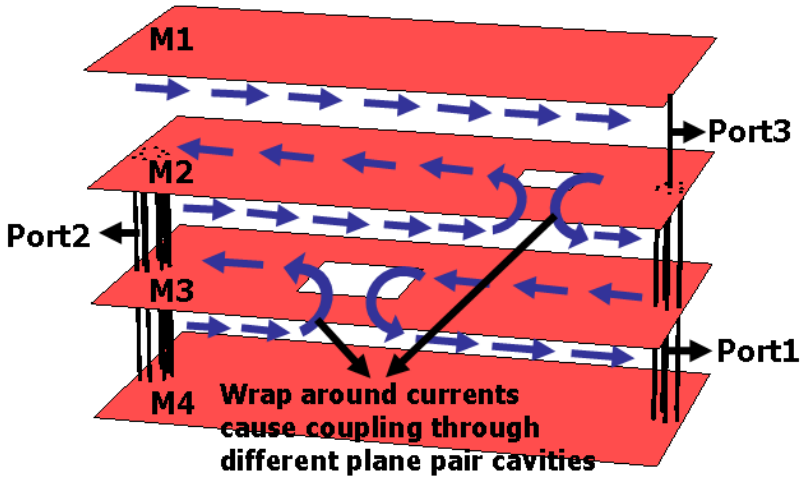


Figure 55 Four metal layer structure with cavity-cavity coupling

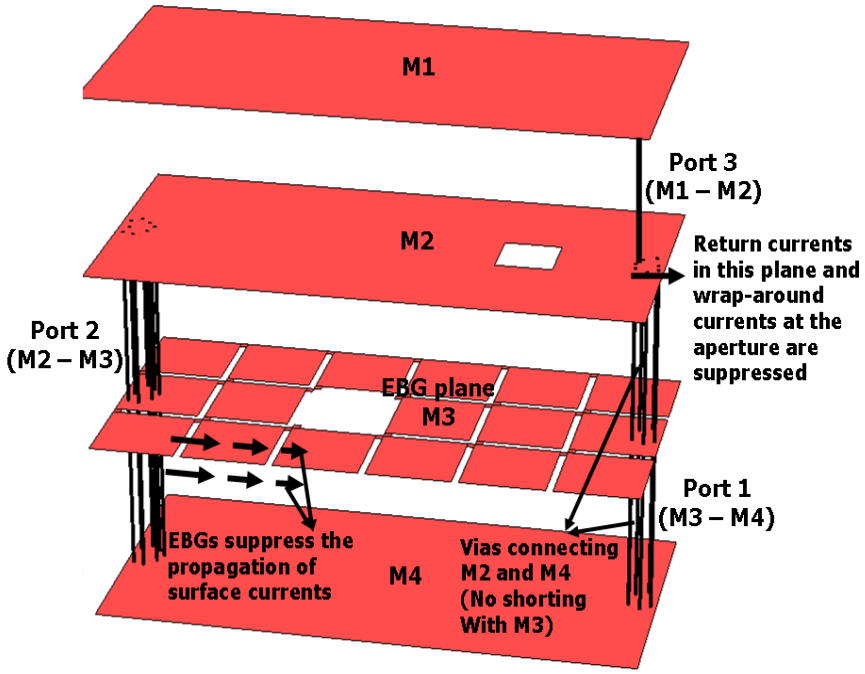


Figure 56 Four metal layer structure with EBGs

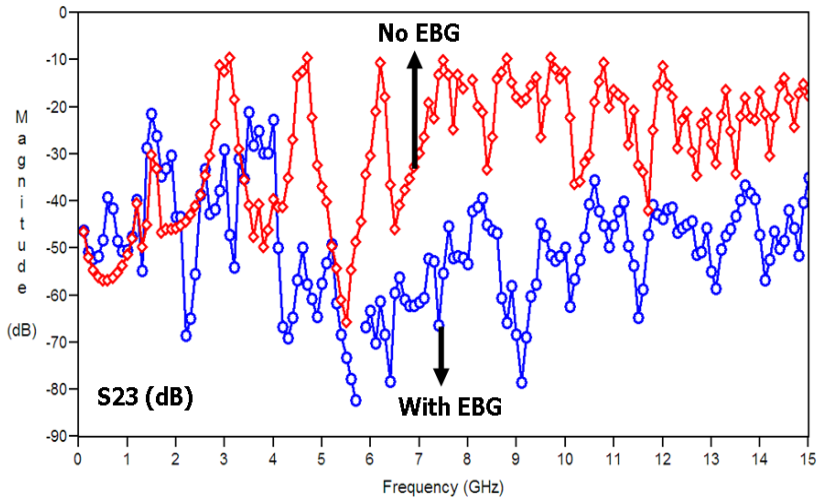


Figure 57 Comparison of results for four-metal layer structure (dB)

3.3. Validation of Vertical Coupling Suppression Method by Measurements

This section discusses the hardware prototypes that were fabricated to demonstrate the suppression of vertical coupling in multilayer substrates through measurements. For the verification of vertical coupling suppression method, a test vehicle was fabricated using FR–4 material. The cross-section of the test vehicle substrate stack-up is shown in Figure 58. The dielectric constant is 4.6 and loss tangent is 0.01.The test vehicle is a four metal layer structure (M1–M4) consisting of individual coupons of different sizes. The S-parameter measurements presented in this section are obtained using a VNA and the measurements are performed using Ground-Signal-Ground (GSG) 500 um pitch air coplanar probes.

Figure 58 Substrate layer stack-up of Test vehicle

In the test vehicle, layers M1 through M3 are used, while M4 has no metallization. M1 and M3 layers are shorted by vias and M2 layer is patterned with EBGs. The vias shorting M1 and M3 do not touch M2. Port 1 (i.e., the excitation) is defined between layers M2 and M3, and Port 2 (i.e., the response) is defined between layers M1 and M2. Figure 59 shows the top view of the M2 layer that consists of the aperture with EBG patterns of patch size of 12 X 12 mm and branch size of 1 X 1 mm with an aperture size of 8 X 8 mm. For the structure in Figure 59, comparison between the simulated and measured S-parameter without using EBGs is shown in Figure 60, while the case of using the EBGs is shown in Figure 61. As seen from the S21 responses in Figure 61, the coupling between Port 1 and Port 2 is effectively suppressed in the frequency range of 2.3 to 5.5 GHz owing to the use of EBGs. The simulation and measurement results agree reliably and good isolation levels are obtained by the vertical coupling suppression method. This structure validates the vertical coupling suppression method discussed earlier in this chapter.

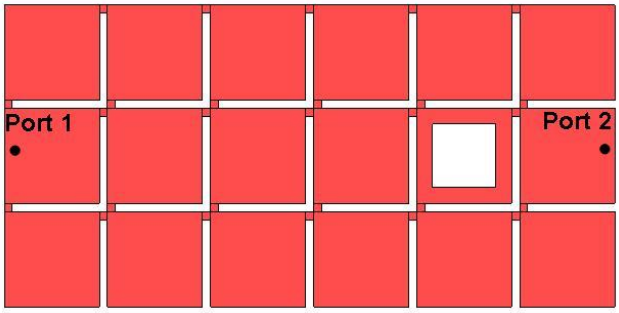


Figure 59 Top view of M2 layer with EBG patterns

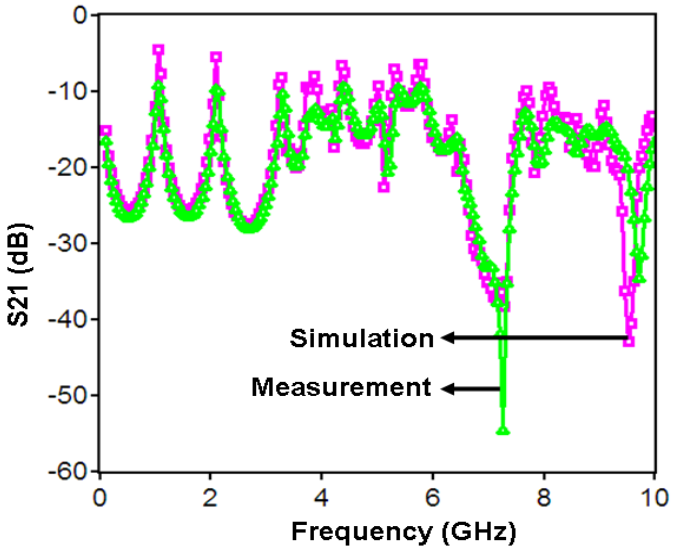


Figure 60 Comparison of simulation and measurement results for the structure in Figure 59 without EBGs

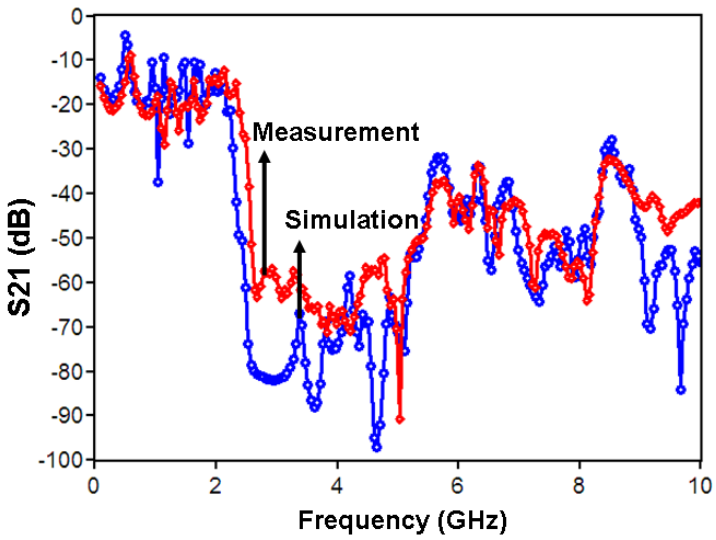
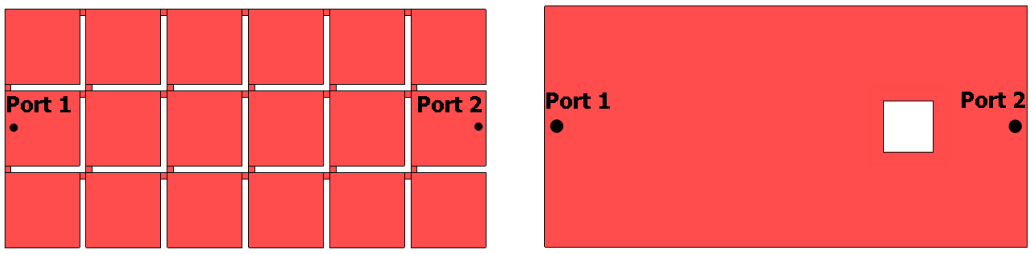


Figure 61 Comparison of simulation and measurement results for the structure in Figure 59 with EBGs

In order to demonstrate coupling suppression across multiple plane pair cavities, another coupon which uses all four metal layers, M1 through M4, was fabricated in the test vehicle in Figure 58. In this coupon, M1 and M4 are solid planes, while M3 is patterned with EBGs and M2 layer contains an aperture of size 7 X 7 mm. The EBG patch size is chosen as 12 X 12 mm and branch size is 1 X 1 mm. M2 and M4 layers are shorted by vias, which do not touch M3. Port 1 (i.e., the excitation) is defined between layers M2 and M3 and Port 2 (i.e., the response) is defined between layers M1 and M2. Figure 62 shows the M3 and M2 layers with Port 1 and Port 2 locations. Figure 63 and Figure 64 show the comparison between simulation and measurement results without and with EBGs, respectively for the structure in Figure 62. As seen from Figure 63 and Figure 64, the vertical coupling suppression method is able to provide isolation across multiple plane pair cavities by patterning one plane with EBG structures.



(a) (b)

Figure 62 Layers (a) M3 and (b) M2 of the 4-metal layer test vehicle coupon

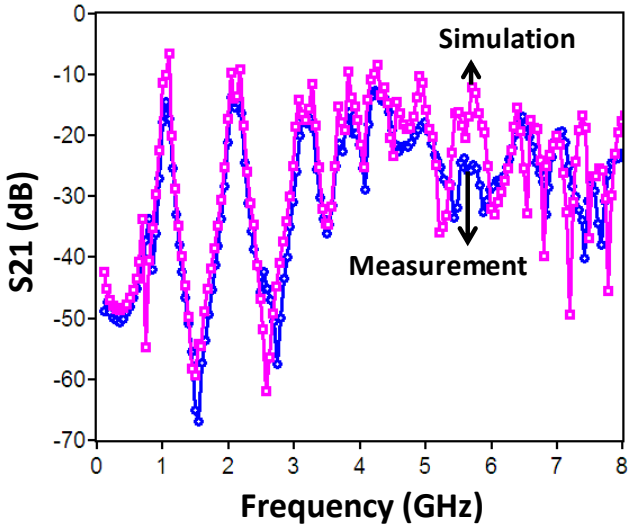


Figure 63 Comparison of simulation and measurement results for the structure in Figure 62 without EBGs on M3

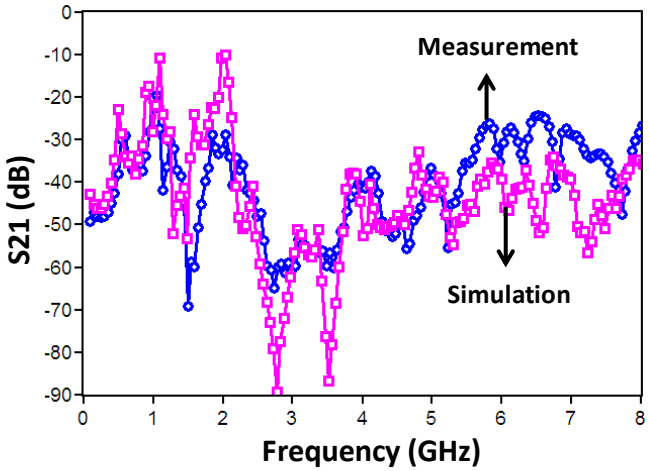


Figure 64 Comparison of simulation and measurement results for the structure in Figure 62 with EBGs on M3

Due to the trend in decreasing package sizes, it is important to study the efficacy of the EBG structures even when the small package sizes only allow for a few EBG unit cells to be fabricated on the power plane. A four metal layer test vehicle was fabricated to study the isolation levels provided by an EBG plane with reduced number of unit cells (i.e., patches and branches). Figure 65 shows the fabricated structure. The dielectric material used is same as the previous test vehicles but the thicknesses of the dielectric build-up layers are different as indicated in Figure 65. The size of a patch is 8 X 8 mm and a branch is 0.5 X 0.5 mm. The lateral dimension of this test vehicle is 25 X 25 mm. Port 1 is defined between Plane 3–Plane 2, while Port 2 is defined between Plane 1–Plane 2. Note that the plane pair cavities across which coupling suppression is measured are not adjacent to the EBG plane (i.e., Plane 3). Also, the number of unit cells in the EBG plane is 3 X 3. The measurement results comparing the structures with and without EBGs are presented in Figure 66. As seen from the figure, the EBGs have suppressed the sharp resonance peaks in the vertical coupling across the plane pair cavities. Figure 67

compares the simulation and measurement results for the above setup. It can be seen that there is a good model to hardware correlation. However, fewer number of EBG unit cells, although suppresses the resonant peaks, results in reduced isolation levels as compared to the previous simulation setup which used 6 X 3 unit cells.

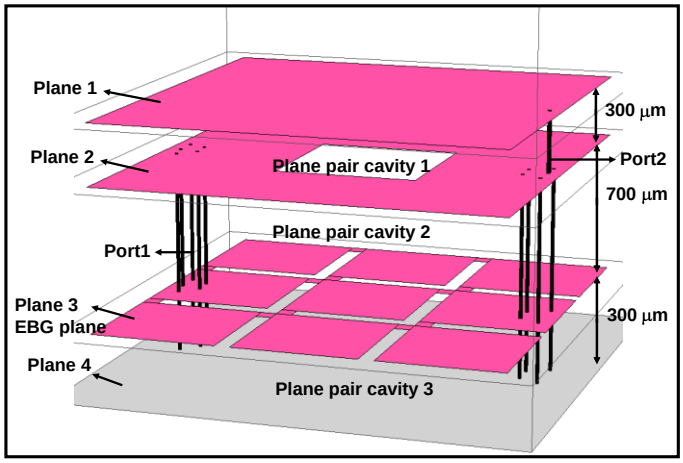


Figure 65 3-D view of the four metal layer test vehicle

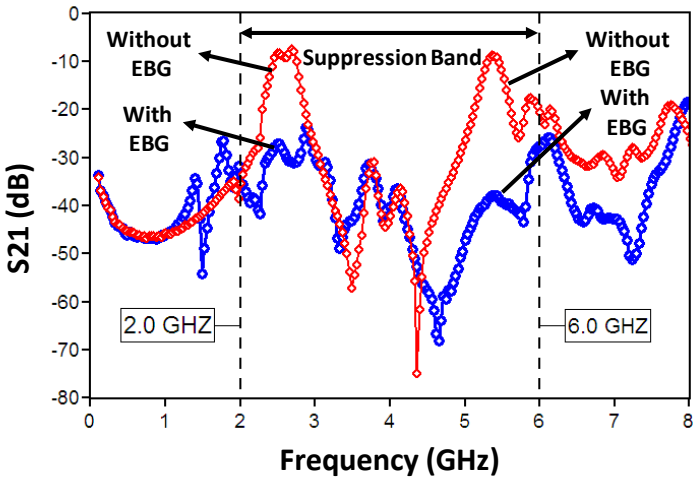
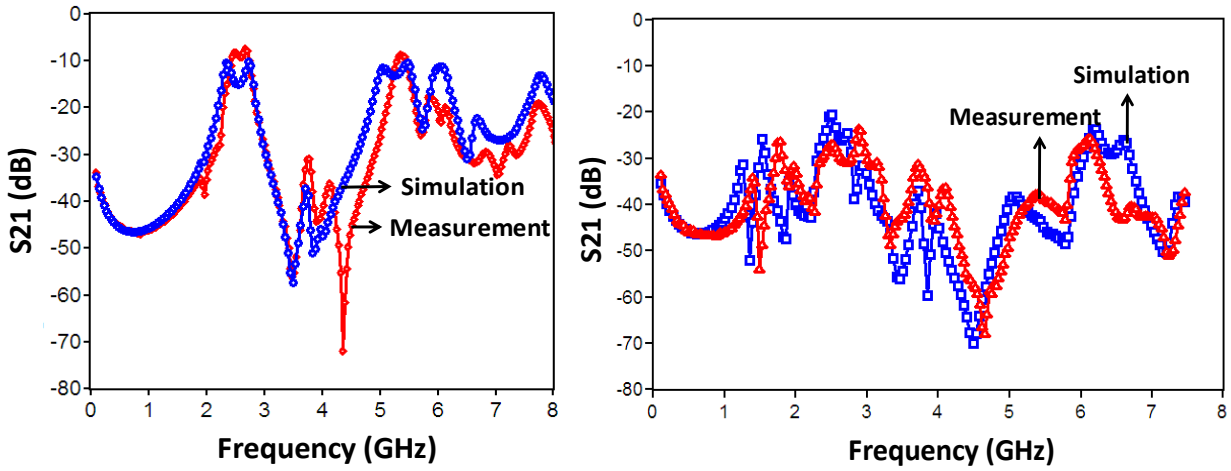


Figure 66 Comparison of results from fabricated four metal layer test vehicle



(a) (b)

Figure 67 Comparison of simulation and measurement results for a) without EBGs b) EBGs

The next hardware prototype demonstrates the suppression of vertical coupling in an embedded actives package. The utility of using an EBG layer here is to provide isolation near the operating frequencies of the embedded die so that the vertical coupling does not affect the proper functioning of the die. The stack-up used for the test vehicle fabrication is shown in Figure 68. A dummy die was used in this case which was placeholder for active die requiring band gap in the frequency region of 3–6 GHz. The prototype consists of a core which is 100 um thick and made up of a material from Rogers Corporation, called the RXP–1. Another variant of this material, called the RXP – 4 is used for the build-up dielectric layers. Two build-up layers are formed on either side of the core. These layers are laminated to form the stack-up as shown in Figure 68. The dielectric constant of RXP–1 is 3.01 and that of RXP–4 is 3.43. The loss tangent is 0.0039 for RXP–1 and 0.0043 for RXP–4. RXP–1 is a glass reinforced hydrocarbon polymer with high glass transition temperature (Tg) and low profile copper cladding

[**100**]. These core materials utilize thermosetting hydrocarbon-based resin system, smooth copper foil for improved loss performance, and flat glass reinforcement to minimize the effect of the glass weave on signal propagation. The laminate material RXP–1 has excellent thermal stability with Tg > 3000° C making it ideal for lead-free solder and other high temperature interconnects. It also has X-Y Coefficient of Thermal Expansion (CTE) in the range of 10–15 ppm/°C. This helps to reduce the stress on first level interconnects from Silicon and other ICs. RXP–4 is an unreinforced build-up available as free standing film, or as resin coated copper (RCF). These low dielectric constant materials support high signal speeds and the low loss at GHz frequencies makes them suitable for RF applications. Some of the other advantages of these organic substrate materials are: 1) light weight and extremely low profile, 2) low cost, 3) high reliability and 4) scalable to large panel processes.

In this prototype, a cavity is made using laser drilling process between the layers M1 and M2. Note that the cavity is not step shaped as was the case in the test vehicle described in Chapter 2. The laser cavity process overcomes the drawback associated with the side walls of the cavity as was the case with photo cavity process. The substrate bond pads for the die are present in layer M2. The embedded die is 7 X 7 mm in size, thinned down to 60 um and consists of a single metallization layer with daisy chain structures. Figure 69 shows multiple coupons with chips embedded within cavities. The S-parameter measurements are obtained using a Vector Network Analyzer (VNA) and the measurements are performed using GSG 500 um pitch Air Coplanar Probes. Figure 70 shows the measurement setup. Figure 71 is the 3D view of the fabricated prototype, while Figure 72 is the top view of the layout showing the EBG patterned M2 layer and the solid

M1 layer. Both these layers house an aperture of size 8 X 8 mm. The size of the module is 25 X 25 mm. The EBG patch size is chosen as 8 X 8 mm and the branch size is 0.5 X 0.5 mm. Slots of length 4 mm and width 0.5 mm are made on the patches as shown in Figure 71 in order to reduce the on-set frequency of the primary (fundamental) band gap of the EBG structures [**101**] to the desired 3–6 GHz range of isolation, while maintaining the package size at 25 X 25 mm. Note that synthesizing suitable EBG unit cells that provide isolation in the desired band gap is important for the efficient implementation of this coupling suppression technique. One such method for fast synthesis of EBGs given the isolation band requirement is described in Chapter 4. Figure 73 compares the measured result from this prototype for the cases - with and without EBG patterns on M2 layer. As seen from the graph, the presence of EBG structures offers deep and wide band isolation in the frequency range 3–6 GHz.

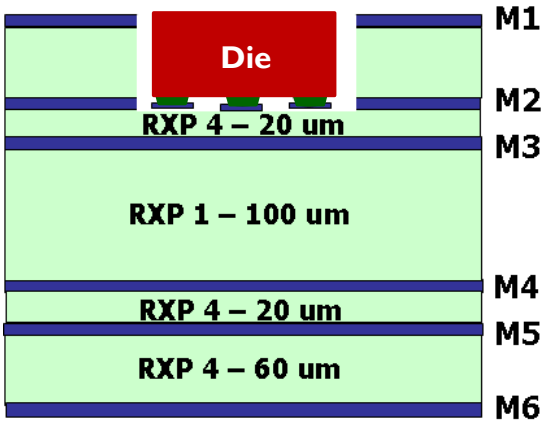


Figure 68 EMAP Active TV — 6 metal layer stack-up

Figure 69 Test Vehicle Coupons with Power/Ground planes and Die embedded within the cavity

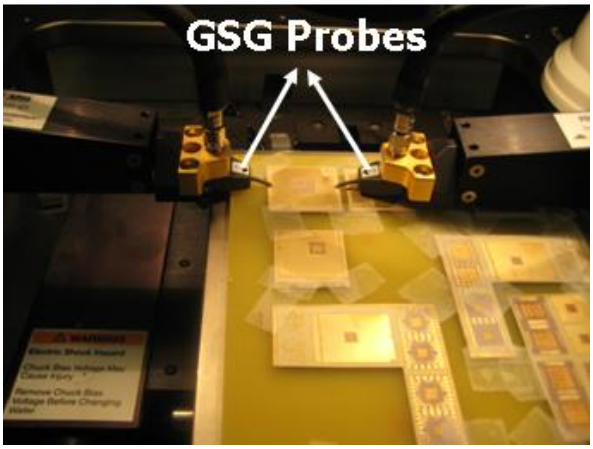


Figure 70 Measurement Set-up with Air Coplanar probes

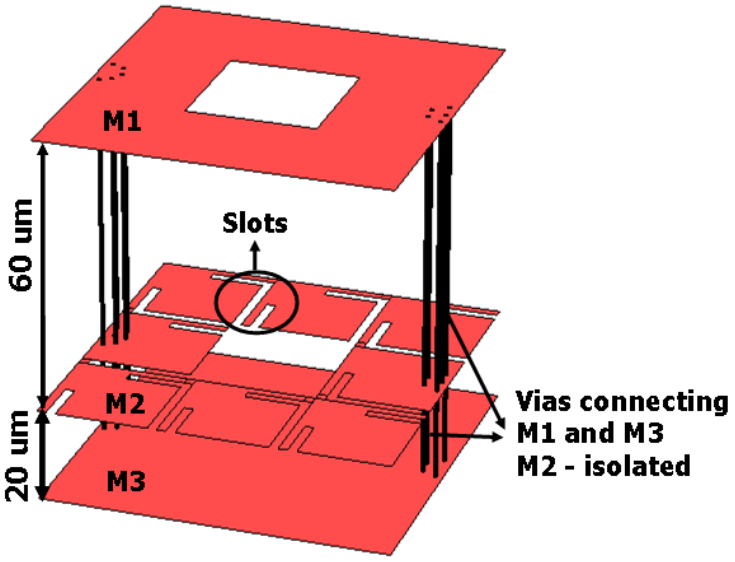
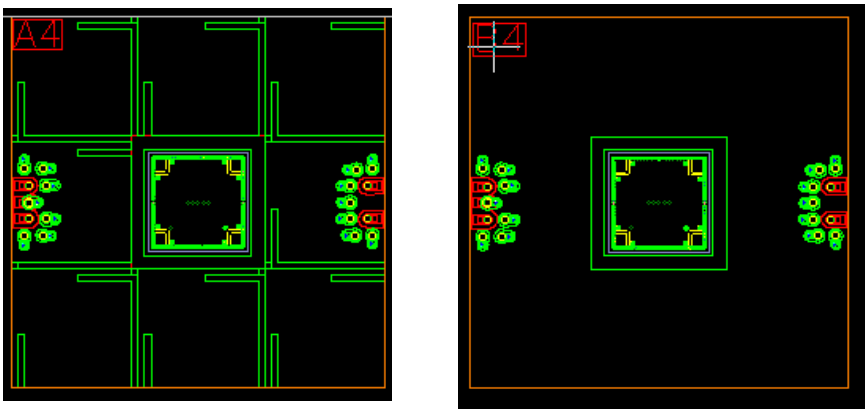


Figure 71 3D view of the multilayer structure with EBG



(a) (b)

Figure 72 Layout of layers a) M2 showing EBG b) M1

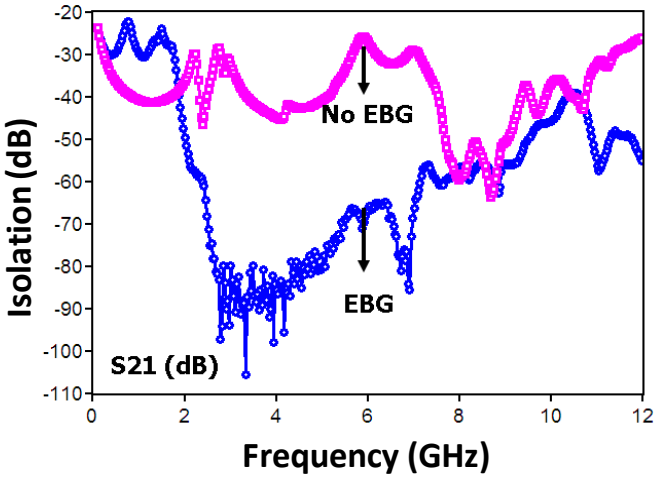


Figure 73 Comparison of measured results from structures with and without EBG

3.4. Concluding Remarks

To conclude, this chapter presented an efficient method for suppression of vertical electromagnetic coupling in multilayer packages with embedded ICs. The effectiveness of the approach was shown to hold good extending into the GHz range where commonly used methods such as split planes and decoupling capacitors are ineffective. The presence of apertures in the power and ground planes of multilayer packages causes EM waves to fringe through the aperture from one plane pair cavity to another as explained in Chapter 2. To counteract the vertical coupling, the plane which had an aperture in the multilayer structure was patterned to form EBG structures. This vertical isolation concept was also extended to provide isolation in plane pair cavities, which were not adjacent to the patterned EBG plane. Test vehicles were fabricated with different layer stack-up and with embedded chip. The simulations performed were validated using the measurement results from the test vehicles to demonstrate the coupling suppression technique.

CHAPTER 4

STOP-BAND PREDICTION FOR ELECTROMAGNETIC BAND GAP STRUCTURES IN MULTILAYER PACKAGES

The design methodology discussed in Chapter 3 addressed vertical coupling suppression by suitably patterning certain power planes with EBG structures in multilayer substrates. In order to implement this technique for real systems, it is important that the isolation achieved using EBGs should target certain frequency bands depending on the needs of the application. Hence, an EBG design methodology which outputs EBG configurations that provide isolation over desired frequency bands is necessary. Moreover, this methodology should be fast as well as computationally inexpensive to be successful. There are several methods available for designing 2-layer EBGs, i.e., EBGs offering isolation within a single plane pair cavity [**102**] [**103**] [**95**] [**104**] [**105**]. In the following, these methods will be described briefly and the need for a fast and efficient synthesis methodology for EBGs is motivated. Subsequently, this chapter describes a synthesis methodology for designing EBGs to address multilayer EM coupling.

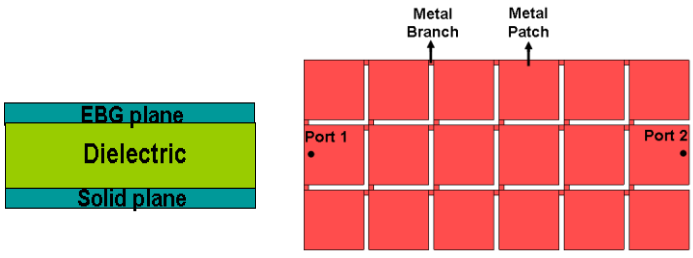


Figure 74 Two layer EBG structure showing the cross-section (left) and the top view of the EBG plane (right)

Full wave EM simulations can be used for characterizing entire EBG planes. In particular, they compute S-parameter responses for the EBG structures using which the isolation frequency bands can be deduced. For example, the structure shown in Figure 74 can be simulated using an EM solver with the excitation and response locations indicated in the figure as Port 1 and Port 2. The S-parameters (dB scale) obtained from the EM-solver give an indication of the magnitude of isolation that can be achieved. Moreover, the Z parameters obtained from the EM solver indicate the transfer impedance across the EBG plane between Port 1 and Port 2 locations. However, this method which involves simulating the entire structure is prohibitively expensive both in terms of computation and time. Methods such as [**95**] [**106**] therefore resort to stop-band prediction based on EBG unit cell, thus avoiding having to simulate the entire EBG plane. These methods rely on the assumption that the EBG plane is obtained by repeating the unit cell infinitely. However, since the actual EBG plane is finite in nature, these methods are limited in their ability to accurately predict the stop bands.

Full wave EM solvers can perform Eigen mode analysis on the unit cell of the EBG structure by using periodic boundary assignment [**107**]. The propagation constants along different axes of the unit cell can be calculated using full wave solver. In periodic structures, the propagation vectors are unique within a certain region of the unit cell called the Brillouin zone and they are redundant outside that region. As an example, the Brillouin zone for a square unit cell of side *d* is shown in Figure 75. Characterizing the propagation constants within a single unit cell, along the boundaries of the Brillouin zone is sufficient to describe the wave propagation behavior of the entire periodic structure formed by these unit cells. In the case of an EM full wave solver, even the Eigen mode

analysis performed on a single unit cell using the solver is still computationally expensive [**108**].

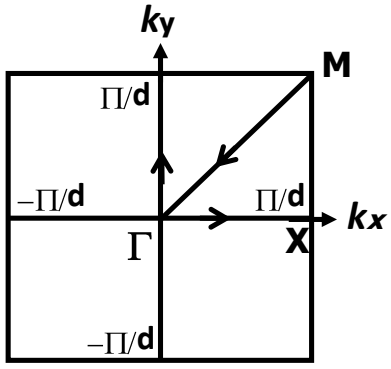


Figure 75 Brillouin zone for a unit cell of square shape and size *d*

In [**95**] [**102**] [**93**] [**109**] [**110**] equivalent transmission line circuit models representing the EBG unit cell have been used to estimate the pass band and stop band frequency ranges. Transmission line circuit models can give a quick estimation of the pass bands and stop-bands if the EBG structures are represented by accurate circuit models, which could be a difficult proposition. Moreover, the circuit models are convenient to formulate only a one-dimensional (1D) Eigen value equation along the principal direction of wave propagation for the prediction of stop bands. In structures where the propagation of electromagnetic waves is anisotropic, this method does not give an accurate estimation [**106**].

In [**106**], a method that remedies the above mentioned drawbacks of [**95**] is proposed. This method involves solving a two-dimensional (2D) Eigen value equation for predicting the pass bands and stop-bands and has been primarily applied on two metal layer Alternating Impedance – Electromagnetic Band Gap Structures (AI-EBGs). Figure 76 shows the unit cell for AI-EBG where‘d’ is the periodicity of the EBG unit cells. The

Brillouin zone for such a unit cell is similar to Figure 75. The limiting sides of the Brillouin triangle are Γ–X, X–M and M–Γ. The co-ordinates of the triangle are, Γ (0, 0), X (π/d, 0) and M (π/d, π/d), where *d* is the periodic interval of the EBG structure as shown in Figure 76. The phase constant is evaluated along Γ–X, X–M, and M–Γ for different frequencies. Bloch's theorem [**111**] describes the nature of wave propagation in periodic structures/crystals. According to this theorem, in an infinite periodic structure of periodicity *d*, the fields in adjacent unit cells, E(x) and E(x + d), differ by a constant attenuation and phase shift, which is captured by the equation below where $\boldsymbol{\gamma}$ is the propagation constant.

$$E(x+d) = E(x) * e(\pm \gamma d) \qquad (1)$$

Consider 2-dimensional wave propagation in X and Y directions of the EBG structure, such that the propagation constants in X direction is $\boldsymbol{\gamma_x}$ and in Y direction is $\boldsymbol{\gamma_y}$. The general solution for a wave propagating in the +X direction in a medium is $\mathbf{e^{-\gamma x}}$, where the propagation constant is $\boldsymbol{\gamma = \alpha + j\beta}$, such that $\boldsymbol{\alpha}$ is the attenuation constant and $\boldsymbol{\beta}$ is the phase constant. Assuming material losses to be zero ($\alpha = 0$), we have $\mathbf{e^{-j\beta x}}$. Now, considering a periodic interval of *d* for the EBG cells in X and Y directions, the fields in the adjacent unit cells differ by a factor of $\mathbf{e^{-j\beta xd}}$ and $\mathbf{e^{-j\beta yd}}$ in the X and Y directions, respectively. A single unit cell of the two-dimensional EBG structure, shown in Figure 76, is represented by a 4 port network for the derivation of Eigen value equation. Voltages and currents at the 4 port locations form the input and output variables, which are represented in terms of transmission (ABCD) parameters in the Eigen value equation.

The derivation of the equation is explained in detail in [**106**]. This equation is solved for X and Y direction propagation constants (i.e., β_x and β_y) at different frequencies and the stop bands and pass bands are predicted based on the solutions obtained. The frequency regions for which a solution of the Eigen value equation cannot be obtained are the stop bands, while the regions where the equation converges and the phase constants can be determined are the pass bands. The Eigen-value equation for the 2D wave propagation in the EBG structure is given by:

$$\left\{\begin{pmatrix} \overline{\overline{F_{11}}} & \overline{\overline{F_{12}}} \\ \overline{\overline{F_{21}}} & \overline{\overline{F_{22}}} \end{pmatrix} - \begin{pmatrix} e^{\gamma x d}\,\overline{\overline{I}} & 0 \\ 0 & e^{\gamma y d}\,\overline{\overline{I}} \end{pmatrix}\right\}\begin{pmatrix} \overline{X_0} \\ \overline{Y_0} \end{pmatrix} = 0 \quad (2)$$

where, ***F*** matrix represents the 4 port transmission parameters, ***I*** is a 2 X 2 unit matrix and ***X0***, ***Y0*** are output vectors containing voltage and current elements. The results from the Eigen value equation can be illustrated with the help of frequency (GHz) versus phase constant plots which indicate the stop bands and pass bands based on the phase constant values. This plot of Frequency vs. Phase constant is called the dispersion diagram and is shown in Figure 77, where the regions shaded in grey correspond to stop bands, while the regions that are not shaded indicate the pass bands. In other words, wave propagation is characterized by varying phase constant with respect to frequency in the pass bands.

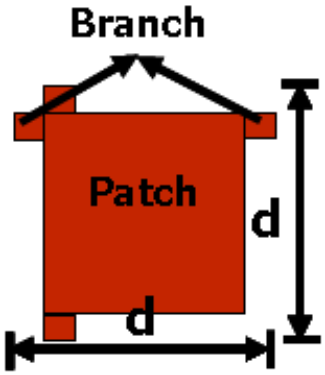


Figure 76 AI-EBG unit cell

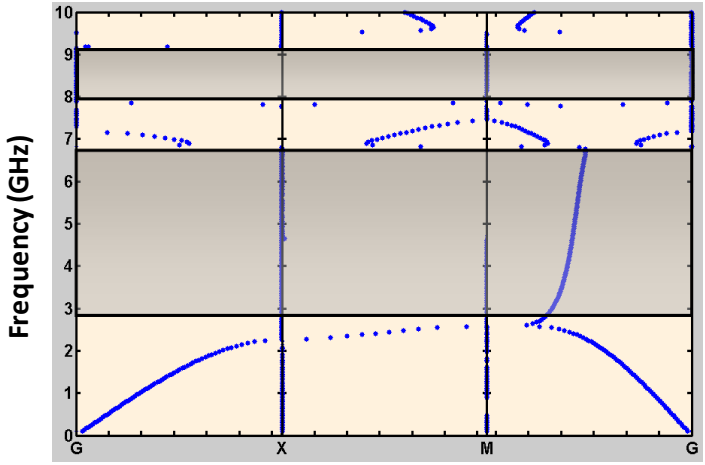


Figure 77 β-f plot for a two-metal layer EBG structure showing the regions (shaded in gray) where EM waves are suppressed

The 2-D dispersion diagram method provides a fast prediction of the band gap for an EBG structure, whose dimensions are provided as inputs. An EM solver is first used to compute the S or Z parameters of the EBG unit cell and using the extracted parameters, the phase constants are evaluated numerically as in the discussion above. Most of the computation time involved in estimating the EBG band gap arises from performing an EM simulation on the unit cell to extract the S or Z parameters, although this is still faster

than performing a fully fledged Eigen mode analysis on a unit cell using an EM solver. The numerical computation part which involves computing the phase constants using the ABCD parameters of the unit cell is not very computationally intensive, and can be performed fast.

The methods described so far involve various methodologies for EBG analysis but they all are analytical methods in the sense that they are designed to predict the stop bands only if the dimensions of the EBG are known a priori. In other words, these methods are not adept when it comes to actually synthesizing EBGs for a given isolation band but can predict the isolation bands if the dimensions of the EBGs are provided. From a mixed signal system design perspective, it is more preferable to be able to synthesize EBG structures that provide band gap in the desired frequency range. In [**112**] a genetic algorithm based approach is used to synthesize EBGs. This method requires the user to provide initial starting dimensions (i.e., hint) for the EBG unit cell after which it uses genetic algorithm in conjunction with dispersion diagram method [**106**] to prune the search space and converge to the appropriate EBG unit cell dimensions. The performance of this algorithm is sensitive to the quality of the initial estimate (i.e., hint), not to mention that the method can get computationally expensive.

In the case of methods that use full wave EM solvers for EBG band gap prediction, the simulation complexity in terms of computational effort and time increases many fold especially when applied to multilayer packages. Hence, it is not a good idea to use a trial and error method in invoking EM solvers to arrive at suitable EBG dimensions that provide a stop band in the required band gap frequency range. In this section, a synthesis method for EBGs is presented which does not make use of the EM solvers. The

method provides a fast preliminary estimate of the EBG unit cell dimensions given the desired band gap frequency range as inputs. Once the preliminary estimate is obtained, a dispersion diagram based method is proposed to obtain the pass bands and stop bands by constructing a multilayer unit cell using the EBG dimensions obtained from the EBG synthesis method.

4.1. EBG Synthesis Methodology Using Stepped Impedance Resonators

An EBG synthesis methodology is now described that produces AI-EBG unit cells satisfying the required band gap specification expressed in terms of a lower stop band frequency f1 and an upper stop band frequency f2. The fundamental band gap is the frequency range in which maximum isolation is provided by the AI-EBG. Any application that requires noise isolation in f1–f2 frequency range would use AI-EBG unit cells whose primary band gap overlaps this frequency range. As the EBG synthesis methodology does not require the use of EM solvers, it can be characterized as a numerical method. Since this methodology is entirely a numerical method, the computation is sensitive to the shape of EBG structure (owing to the dependence of the wave propagation characteristics on the EBG shape), which means that it is difficult to generalize this method for any configuration of EBGs (i.e., any EBG unit cell other than AI-EBG). The analysis takes f1 and f2 as inputs and produces several possible dimensions of EBGs (i.e., dimensions of patch and branch) that provide isolation in the frequency range f1–f2. There are a few additional inputs to the analytical (numerical) model, such as the properties of the dielectric material as well as those of the fabrication process, which are discussed later in the section. Note that the analytical model treats f1

and f2 as mere guidelines and tries to find suitable EBGs that would provide isolation between these frequency ranges but some of the outputs may span larger isolation bands containing f1 and f2. For example, if f1 is 1 GHz and f2 is 2 GHz, the model could also output EBG dimensions as answers that provide isolation between 0.5–3 GHz, which, as one could notice, still meets the input specification.

The analytical model for the synthesis of EBGs is based on modeling them as Stepped Impedance Resonators (SIRs). SIRs are widely used for various configurations of filters, ring resonators, hairpin resonators, to name a few [**113**] [**114**] [**115**] [**116**] [**117**]. SIRs consist of cascaded sections of transmission lines of different characteristic impedances [**118**]. Figure 78 shows SIRs consisting of cascaded sections of transmission lines with characteristic impedances Z1 and Z2, which are of electrical lengths $\vartheta 1$ and $\vartheta 2$, respectively. Let K be the impedance ratio of the SIR given by Z1/Z2. The idea behind EBG synthesis using SIRs is that they are used in the realization of band pass and band stop filters [**119**] [**114**] based on the resonance and anti-resonance properties of the cascaded sections forming the SIR. As explained before, EBG structures also exhibit pass bands and stop bands, and this similarity in behavior motivates the use of SIRs as the fundamental elements in EBG synthesis. When modeling EBGs as SIRs, the rejection provided by the SIRs between the 1^{st} and 2^{nd} resonance frequency points forms the fundamental band gap of the EBG structure.

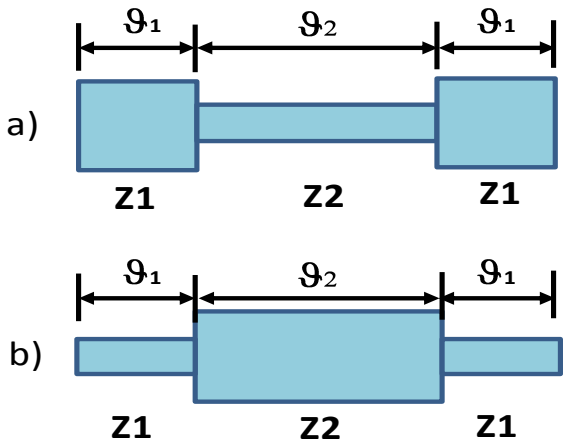


Figure 78 SIR with a) K<1 and b) K>1

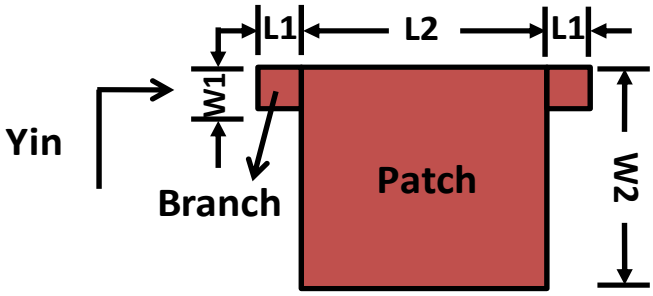


Figure 79 AI-EBG unit cell as SIR

Figure 79 shows a unit cell of AI-EBG, which is treated as an SIR. The branch of the AI-EBG corresponds to the Z1 segment of the SIR, while the patch corresponds to the Z2 segment of the SIR. The AI-EBG unit cell is characterized by branch and patch of length L1 and L2, and width W1 and W2, respectively. This unit cell is repeated continuously throughout the EBG plane. The resonance conditions of the unit cell are derived by treating it as an SIR and estimating the fundamental stop band of the EBG as detailed above. The input admittance, Yin, of the unit cell looking into it as shown in Figure 79 is given by equation (1) and (2) below:

$$Zin = jZ2\left(\frac{(-Z1*Z2*\cot\theta 2)+(Z1^2*\tan\theta 1)+(Z1*Z2*\tan\theta 2)+(Z2^2*\tan\theta 1)}{(Z1*Z2)+(Z2^2*\tan\theta 1*\cot\theta 2)+(Z1*Z2*\tan\theta 2*\cot\theta 2)-(Z1^2*\tan\theta 1*\tan\theta 2)}\right) \quad (1)$$

$$Yin = \frac{1}{Zin} \quad (2)$$

where *Zin* is the input impedance and *Yin* is the input admittance.

At resonance, the input admittance of the unit cell structure becomes zero resulting in infinite input impedance to the propagation of electromagnetic waves through the structure. The first resonance of the structure is the frequency at which the input admittance passes through zero when performing a frequency sweep. This denotes the beginning of the fundamental band gap. Similarly, resonance immediately following the fundamental resonance where the admittance once again crosses over zero signifies the end of the band gap. At resonance, equation (1) reduces to:

$$2 * K * \tan(\theta 2) + K^2 * \tan(\theta 1) - \tan(\theta 1) * \tan^2(\theta 2) = 0 \quad (3)$$

where K = Z1 / Z2 is the impedance ratio of the unit cell. In order to estimate the electrical lengths of the AI-EBG patch (i.e., $\vartheta 2$) and branch (i.e. $\vartheta 1$), the inputs required are the lower f1 and upper f2 limits of the isolation band frequencies of the target application, the dielectric constant ε_r of the dielectric material, the maximum Z1 and minimum Z2 permissible impedances and the thickness t of the dielectric material. The impedances are a function of the fabrication process and determined by the feature sizes that can be fabricated. In particular, the value of Z1 is determined by the smallest feature size that is supported by the fabrication process. It is assumed here that Z1 and Z2 are provided. The electrical lengths $\vartheta 1$ and $\vartheta 2$ are related to the physical dimensions of the EBG unit cell and lower f1 and upper f2 frequency limits by the following family of equations:

$$\vartheta 1 = (2\pi.f1.L1_{max}) / (c.\sqrt{\varepsilon_r}) \;\&\; \vartheta 2 = (2\pi.f1.L2_{max}) / (c.\sqrt{\varepsilon_r}), \quad (4)$$

$\vartheta 1 = (2\pi.f2.L1_{min}) / (c.\sqrt{\varepsilon_r}\,)$ & $\vartheta 2 = (2\pi.f2.L2_{min}) / (c.\sqrt{\varepsilon_r}\,)$, (5)

where c is the velocity of light in m/s. $L1_{max}$ and $L2_{max}$ (which are unknowns) are the branch and patch lengths corresponding to the lower band gap limit. Similarly, $L1_{min}$ and $L2_{min}$ (which are unknowns) are the branch and patch lengths corresponding to the upper band gap limit. Moreover, $L1_{max}$ & $L1_{min}$ and $L2_{max}$ & $L2_{min}$ form the bounds for the branch and patch lengths, respectively. The patch length of the EBG unit cell cannot be smaller than $L2_{min}$ as well as cannot be larger than $L2_{max}$. Similarly, the branch length of the EBG unit cell cannot be smaller than $L1_{min}$ as well as cannot be larger than $L1_{max}$.These values are determined by solving (3) over a large range of values, typically from 0.01 mm to 30 mm. Note that this step computes the lengths of patch and branch corresponding to the lower and upper band gap frequencies independently. In other words, if, $L1_{min}$ and $L2_{min}$ are used as the branch and patch lengths, the resulting AI-EBG will only guarantee band gap at the upper frequency limit. Similarly, using $L1_{max}$ and $L2_{max}$ will only guarantee band gap at the lower frequency limit. The purpose of this iteration as mentioned above is to arrive at an upper and lower bound for the lengths of the patch and branch of the AI-EBG unit cell. This iteration is fairly quick as only two unknowns are computed.

The next step is to determine a branch of length L1 and patch of length L2, which guarantee isolation across both the lower and upper limits of the band gap. Let $f1_{min} = f1 - \Delta$ and $f2_{max} = f2 + \Delta$, where Δ is suitably assumed, typically 1GHz. A MATLAB program is used to vary L1 between $L1_{min}$ and $L1_{max}$, L2 between $L2_{min}$ and $L2_{max}$ and f between $f1_{min}$ and $f2_{max}$. $\vartheta 1$ and $\vartheta 2$ are computed by substituting the values of L1, L2

and f in (4) and (5). The values of $\vartheta 1$ and $\vartheta 2$ are then substituted in (3). As the loop consisting of L1, L2 and f progresses, the first zero transition of the admittance gives the lower frequency limit F1 of the isolation band and the subsequent zero transition gives the upper frequency limit F2 of the isolation band for a given L1 and L2. If F1 <= f1 and F2 >= f2, then, the corresponding L1 and L2 are displayed as output. Table 1 is a sample output of the analytical model. The impedances of the branch and patch with widths W1 and W2 are computed using the characteristic impedance equation for micro-strip line configuration. These are checked against the maximum Z1 and minimum Z2 impedance values provided as input [**120**] to ensure that the synthesized EBG unit cell can be fabricated. The EBG synthesis methodology described so far is captured in the flowchart in Figure 80 and Figure 81.

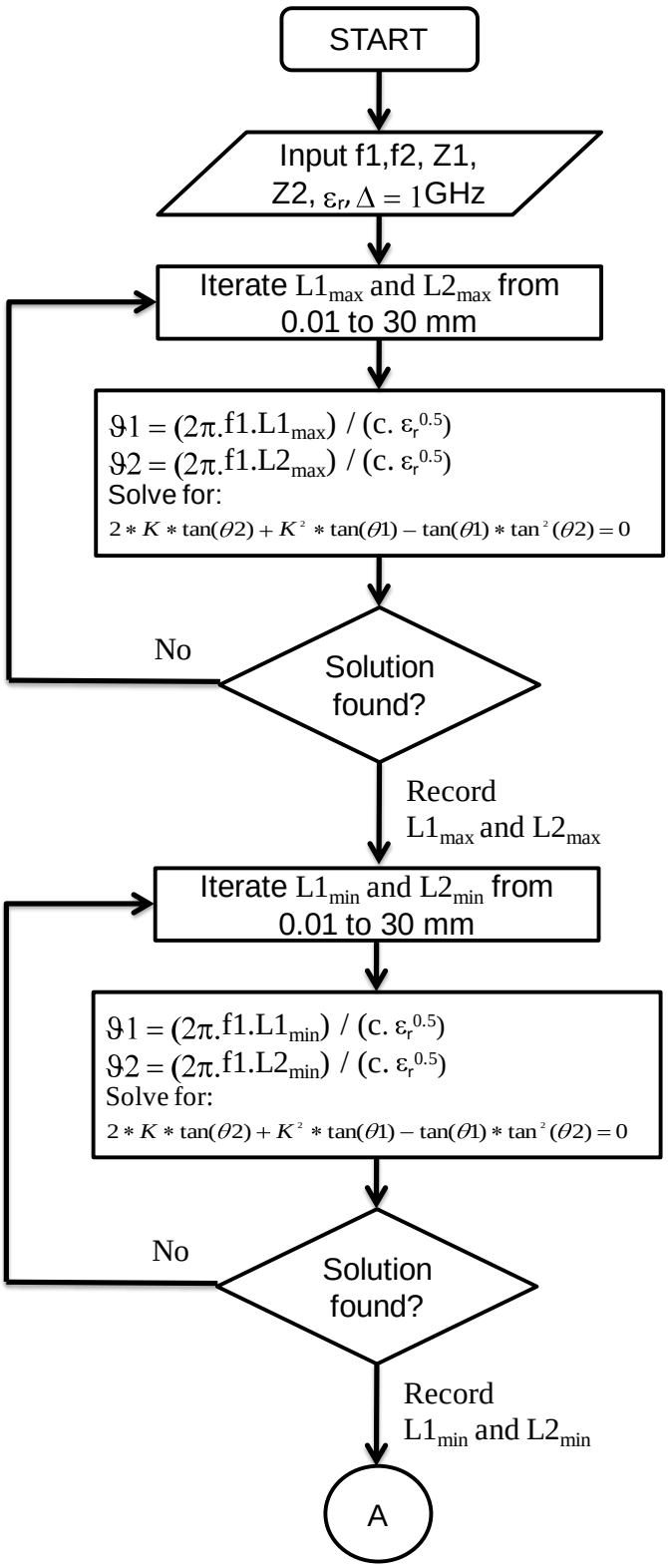


Figure 80 A flowchart of the EBG synthesis algorithm (continued in Figure 81)

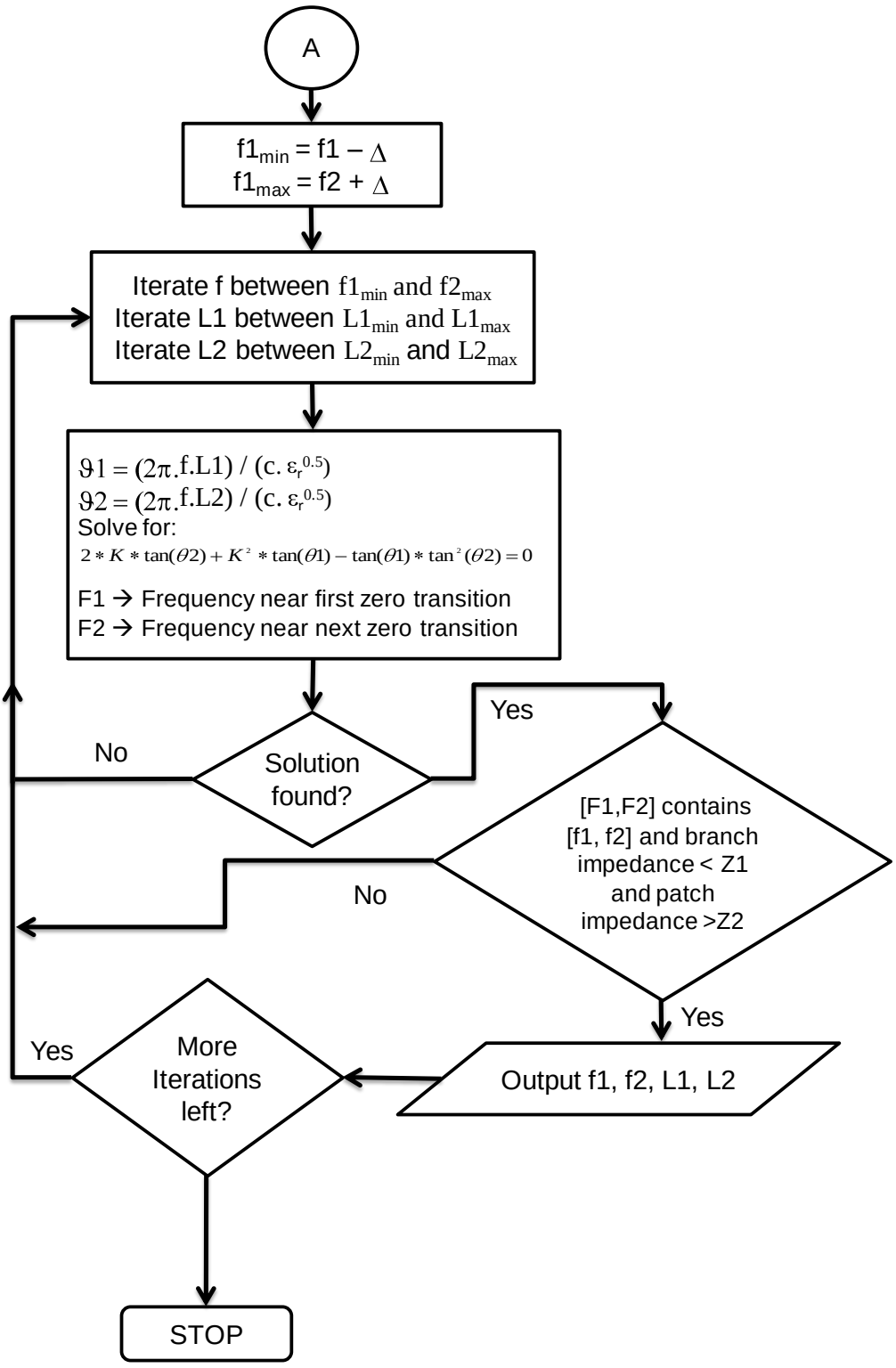


Figure 81 A flowchart of the EBG synthesis algorithm (continued from Figure 80)

4.1.1 Validation of Synthesis Methodology by Simulations

This section discusses the results obtained from the analytical model for different configurations of EBGs, which are compared with the results obtained from EM solver [**121**] and dispersion diagram methods [**106**]. Recall that both EM solver and dispersion diagram methods are not synthesis methods in the sense that they require EBG dimensions as inputs so that they can predict the isolation bands produced. In this section, given a desired isolation band gap as input, the output of the analytical model is used as inputs to the EM solver and dispersion diagram methods to verify if they can reproduce the desired stop bands to give the analytical model a measure of validation. Later in the section, several measurement results drawn from published works is compared with the analytical model results, which provide an even more rigorous validation.

Consider an example where isolation is required from 4 GHz (i.e., f1) to 7 GHz (i.e. f2). The maximum impedance Z1 is 33Ω, while the minimum impedance Z2 is 0.7Ω. The dielectric material used is FR–4, with ε_r of 4.5, loss tangent tan (δ) of 0.01 and thickness t of 0.2 mm. Table 1 is the output from our analytical method containing several synthesized EBG unit cells and the corresponding band gaps they produce, which satisfies the input band gap of 4–7 GHz.

Table 1 Output of Analytical Model

F1 (GHz)	F2 (GHz)	Patch dimension L2 (mm)	Branch Dimension L1 (mm)
3.3	7.94	8.9	0.7
3.28	7.9	8.95	0.7
3.24	7.81	9.0	0.7
3.23	7.77	9.05	0.7
3.21	7.73	9.1	0.7
3.19	7.69	9.2	0.7
3.16	7.6	9.3	0.7
3.13	7.52	9.4	0.7
3.09	7.44	9.5	0.7
3.06	7.37	9.6	0.7
3.03	7.29	9.7	0.7
3.01	7.25	9.75	0.7
2.98	7.18	9.8	0.7
2.95	7.11	9.9	0.7
2.94	7.07	10.0	0.7

From Table 1, the highlighted cases are selected for further validation through electromagnetic simulations and 2D dispersion diagram method [**106**]. EBG planes are formed using patch and branch sizes of (9.1 mm, 0.7 mm) and (9.8 mm, 0.7 mm) and simulated using a tool based on Multilayer Finite Difference Method (MFDM) [**64**]. The number of unit cells used in the EBG plane is shown in Figure 82. Note that the impact of restricting the EBG plane to a finite size in the EM solver model as compared to the analysis which considers the EBG plane to be infinite does not affect the response of the EBG plane significantly as was shown earlier in this chapter. Figure 83 shows the comparison between the EM solver results and the output from the analytical model. This demonstration shows the sensitivity of the analytical model to the variations in patch dimensions, while keeping the branch dimensions fixed. Note that both these cases provide the desired band gap, thereby validating the analytical model.

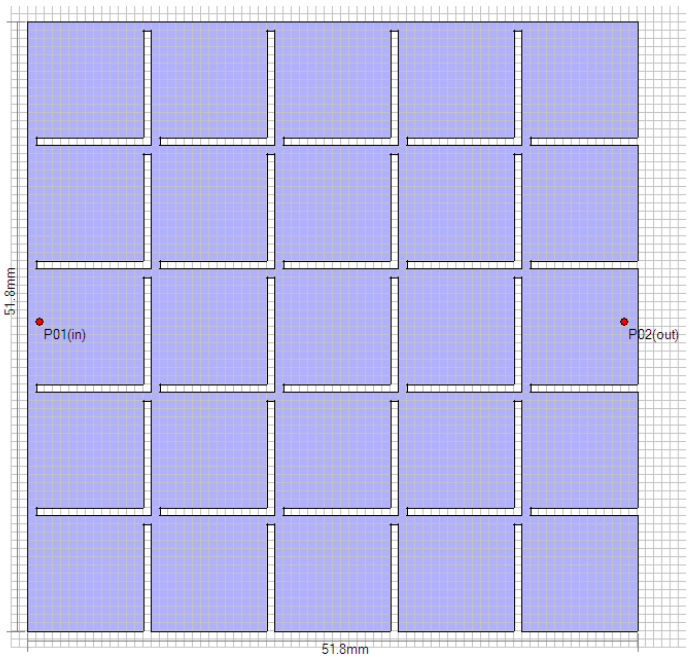


Figure 82 EBG plane used in the EM simulations

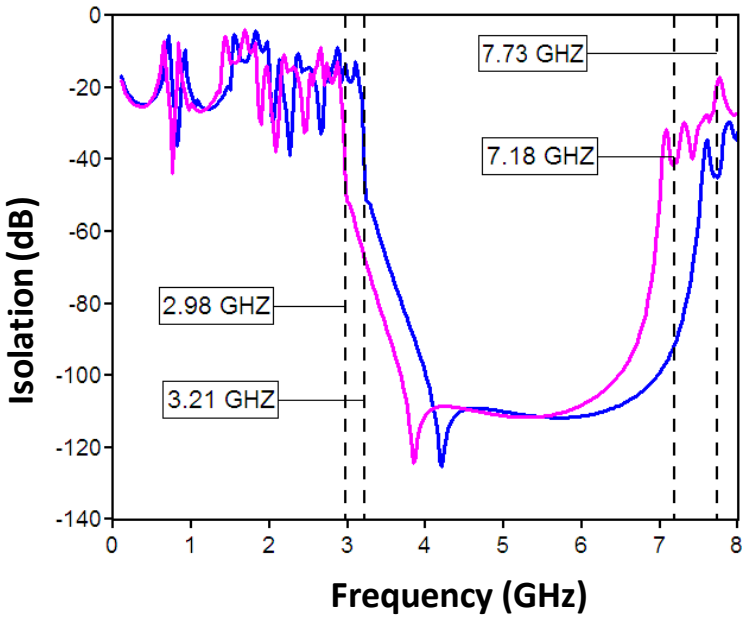


Figure 83 Isolation responses for AI-EBG specifications highlighted in Table 1, where blue and pink curves correspond to patch sizes of 9.1 mm and 9.8 mm.

Figure 84 shows the comparison of analytical modeling results alongside the results from EM simulation and dispersion diagram methods. Notice that the analytical method

and the dispersion diagram method agree only reasonably well as they use different indicators to determine start and end of the band gap. The predicted band gap in the case of dispersion diagram method begins when the propagation constants of the EM wave become indeterminable (i.e., imaginary) and ends when they becomes real once again. However, in the analytical model the band gap starts at the first resonance of the structure (i.e., input impedance becomes infinite) and ends at next resonance. But, in spite of these differences the output of the analytical model satisfies the input band gap specification and agrees well with the EM simulation results. Moreover, the analytical method is also much faster than the other methods. To give an estimation of the speedups obtained using the analytical model, the time taken when the above simulations are performed on a computer with 2GB RAM are: EM solver — 334s, dispersion diagram method — 200.59s, analytical method — 2.81s. The analytical model was found to be over 100X faster than the EM solver and over 70X than the dispersion diagram method, while producing comparable outputs. In the next example a simulation result from literature is validated with the analytical model output.

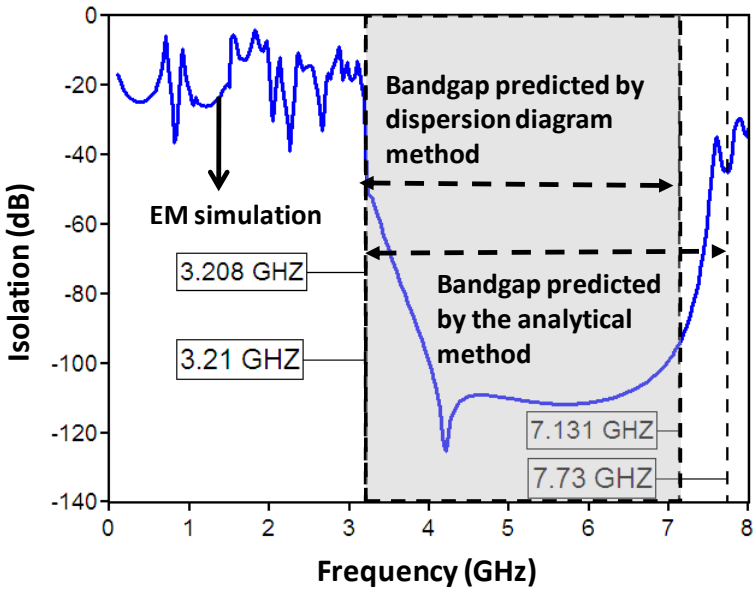


Figure 84 Comparison of EM simulation, k-β plot and analytical model results

This example validates a simulation result from [**122**] against the analytical method. The dielectric material used in [**122**] was FR–4, with ε_r of 4.4, loss tangent tan (δ) of 0.01 and thickness t of 0.3 mm. The EBG used in [**122**] had patch and branch lengths of 14 mm and 1 mm, respectively providing a primary isolation band from 2.3GHz to 5.0 GHz. The maximum and minimum impedances were set to 34.65 Ohm and 0.72 Ohm, respectively. Given these values as inputs, the validation of the analytical model is complete only if the dimensions produced by the model matches those from [**122**]. Table 2 gives the output of the analytical model, which perfectly matches the dimensions of the EBG used in [**122**]. Next, in Figure 85 the simulation result from [**122**] and the analytical model band gap limits are overlaid, thus demonstrating the effectiveness of the analytical model in predicting the fundamental band gap;

Table 2 Output of Analytical Model

F1 (GHz)	F2 (GHz)	Patch dimension (mm)	Branch dimension (mm)
2.11	5.05	14	1

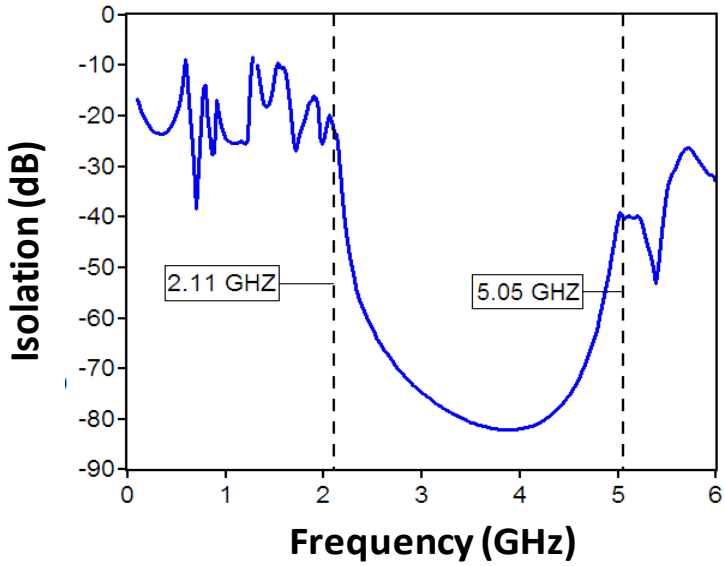


Figure 85 Comparison of simulation result from [122] with the output of the analytical model

4.1.2 Validation of Synthesis Methodology by Measurements

Next, the analytical model is validated against the measurement results from fabricated test vehicles in [**63**] [**123**]. In [**63**], the isolation band is required from 2.5 GHz (i.e., f1) to 4.5 GHz (i.e. f2) for which they used EBG with patch and branch sizes of 15 X 15 mm and 1 X 1 mm, respectively. The dielectric material used was FR–4, which had a dielectric constant ε_r of 4.4, a loss tangent tan (δ) of 0.02 and thickness t of 0.203 mm. Z1 is 26.5Ω, while Z2 is 0.4Ω. The output of the analytical model shown in Table 3

matches the dimensions from [**63**] perfectly.

Table 3 Output of Analytical Model

F1 (GHz)	F2 (GHz)	Patch dimension (mm)	Branch dimension (mm)
1.9900	4.7700	15	0.5

Furthermore, the simulation, measurement and analytical model results are compared with the desired isolation band frequency limits in Figure 86 below. The output from the analytical model meets the input isolation band specifications. The EM simulation and the measurement results agree well with the analytical model.

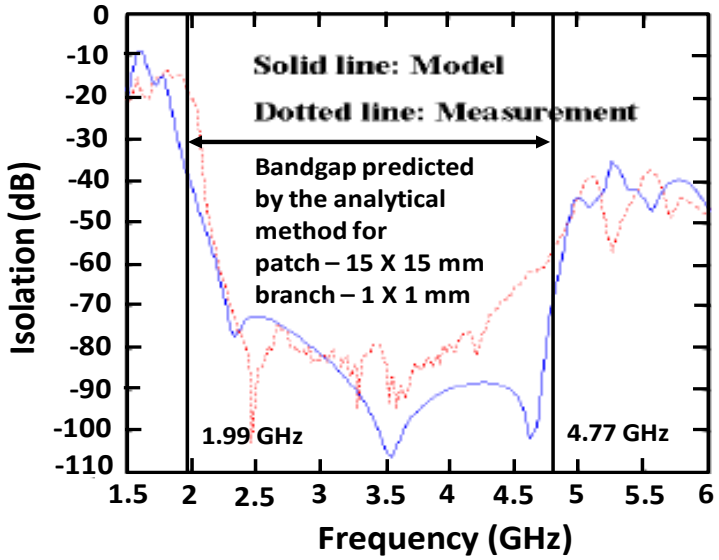


Figure 86 Comparison of results from EM solver, measurement and analytical model

In the final example, the analytical model is applied against a case study from [**123**] to showcase the applicability of the model to real world design scenarios. In [**123**], an EBG plane is used to offer isolation in a mixed signal module, which has FPGA and LNA chips both powered from the same power/ground planes. The LNA operates at 2.4

GHz and good isolation is required in the frequency range around 2.13 GHz to ensure the noise from the FPGA driver does not affect the working of the LNA chip. The dielectric material used in the mixed signal package is FR–4 with ε_r of 4.4, a loss tangent tan (δ) of 0.02 and thickness t of 0.127 mm. Z1 is 53.46Ω, while Z2 is 0.23Ω. The output of the analytical model is given in Table 4. In Figure 87, the output of the analytical model is overlaid on top of the measurement result from [**123**]. Again good agreeement is obtained between the measurement result and the output of the analytical model.

Table 4 Output of Analytical Model

F1 (GHz)	F2 (GHz)	Patch dimension (mm)	Branch dimension (mm)
1.44	3.58	20	2

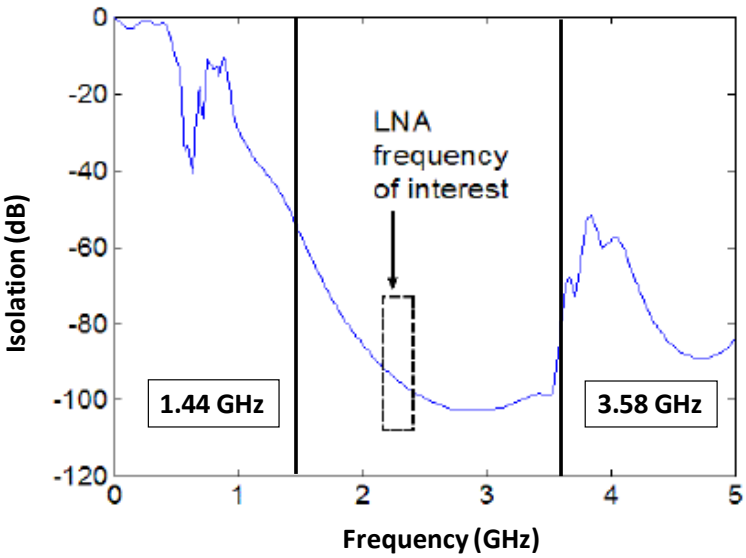


Figure 87 Comparison of simulation result from [123**] with the output of the analytical model**

The simulations and measurement results validated so far using the synthesis methodology demonstrate the efficacy of the approach in estimating the EBG unit cell dimensions based on the input band gap specification. This approach is much faster than existing methods, while producing results of comparable quality. The simplicity of this approach obviates the need to use expensive EM solvers for synthesizing EBGs, which would be valuable from mixed signal system design perspective.

4.2. Prediction of Stop Bands for the Synthesized EBGs in a Multilayer Substrate

This section discusses the prediction of the frequency range of isolation band within which vertical coupling suppression can be achieved in multilayer packages by implementing the EBG unit cells synthesized as described in Section 4.1. The 2D Eigen value method explained in [**122**] is extended to multilayer EBGs. Note that EBGs used in multilayer substrates can effectively suppress coupling in the vertical direction through apertures as shown in section 3.2 of Chapter 3. However, note that if the EBG plane consists of apertures, the periodicity of these EBG structures is lost at the region of the apertures. It is important to properly characterize the vertical coupling through the apertures to evaluate the performance of EBGs in this setting. The substrate stack-up used for simulations presented here is shown in Figure 88. In all the structures discussed in this section, layer M2 is patterned with EBGs. Layers M1 and M3 are connected by vias that do not short the EBG plane (M2). All the EBG structures used throughout this section have a patch size of 8 X 8 mm and a branch size of 0.5 X 0.5 mm. Of course, these patch and branch sizes have been chosen just to demonstrate the prediction methodology using simulations but other sizes of EBGs could also have been used here. Recall that the EBG

synthesis methodology from the previous section works by identifying the fundamental band gap of an EBG structure. But, when it comes to providing vertical coupling isolation in a multilayer package with aperture on the EBG plane, the challenge is in factoring the effect of apertures on the vertical coupling by numerical methods, which is a hard problem. Therefore, in this section a prediction methodology which can compute the pass bands and stop bands of EBG structures with aperture is proposed. The key idea here is to develop a hybrid method that combines the EBG synthesis method with a dispersion diagram analysis that takes in to account the effect of aperture present in the given multilayer stack-up.

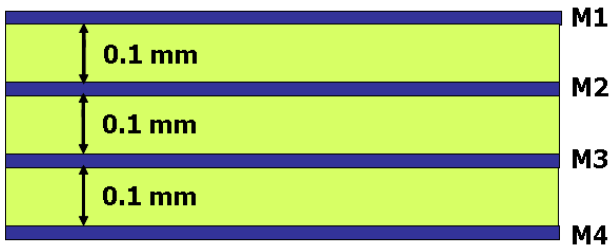
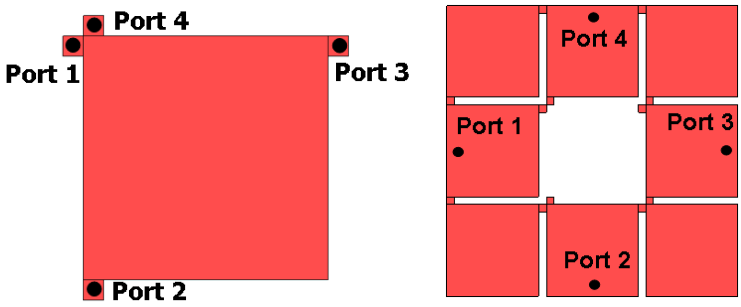


Figure 88 Stack-up used for simulations

Consider rectangular EBG planes with apertures of regular shapes. To effectively predict the isolation in the vertical direction, the unit cell used here is a multilayer unit cell that includes the aperture. Figure 89a shows the unit cells for a two-layer EBG. This EBG contains a solid reference plane below the unit cell, which is not shown in the figure. Next, Figure 89b shows the unit cell for a three-metal layer EBG containing the aperture. The other two metal layers above and below the EBG plane are solid, which is not shown in the figure. The EM wave coupling through the aperture along the two lateral dimensions of the aperture can be characterized using the unit cell shown in Figure 89b. Ports 1–4 are the four ports of the unit cell. In Figure 89a all the four ports are on the

same layer (referenced between EBG plane and solid plane below) and in Figure 89b, Ports 1–2 are defined between M2–M3 layers and Ports 3–4 are defined between M1–M2 layers.



a) b)

Figure 89 a) Two-metal EBG unit cell b) Three-metal layer EBG unit cell

Figure 90 shows the phase constant (β) vs. frequency (f) plot with the regions where electromagnetic wave propagation are suppressed. This plot is obtained by evaluating the phase constants across different frequency regions for the structure in Figure 89b as discussed in [**122**]. This method is applied for band gap prediction of large sized structures shown in Figure 91, where it can be expensive to simulate the entire structure. Figure 91 shows the top view of two structures that have lateral dimensions 42 X 42 mm and 59 X 59 mm. These structures have the same aperture as in Figure 89b. Figure 92 compares the band gap obtained from the β–f plot with the S-parameter response from simulations performed on the structures shown in Figure 91. The multiple graphs shown in Figure 92 are for different port and aperture locations on M2 layer for the structures in Figure 91.

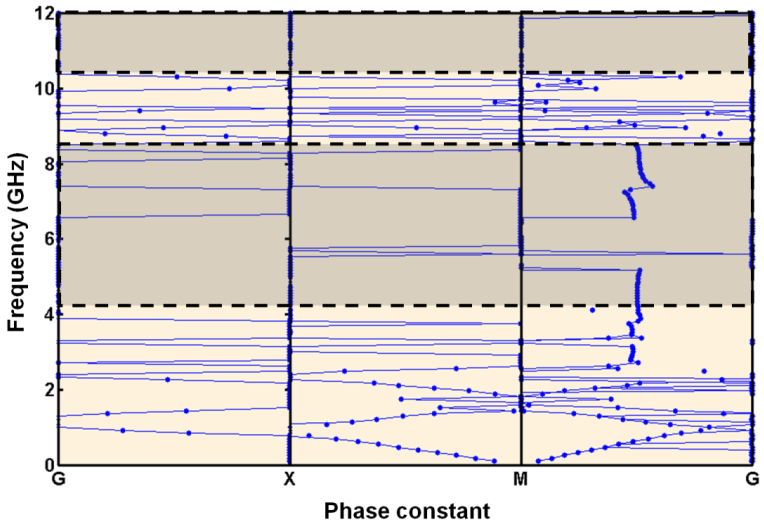


Figure 90 β – f plot showing the regions (shaded in gray) where suppression of vertical coupling is achieved

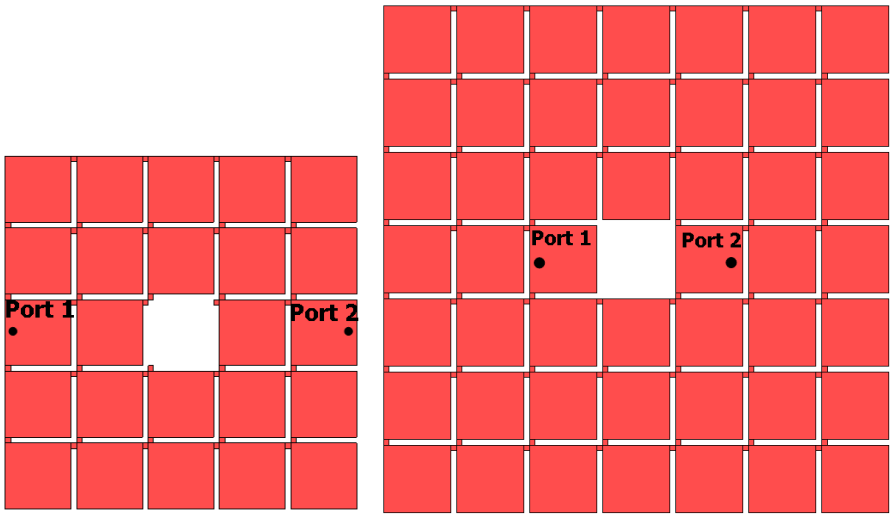


Figure 91 Top View of EBG plane (M2) in three-metal layer structures with port locations as marked

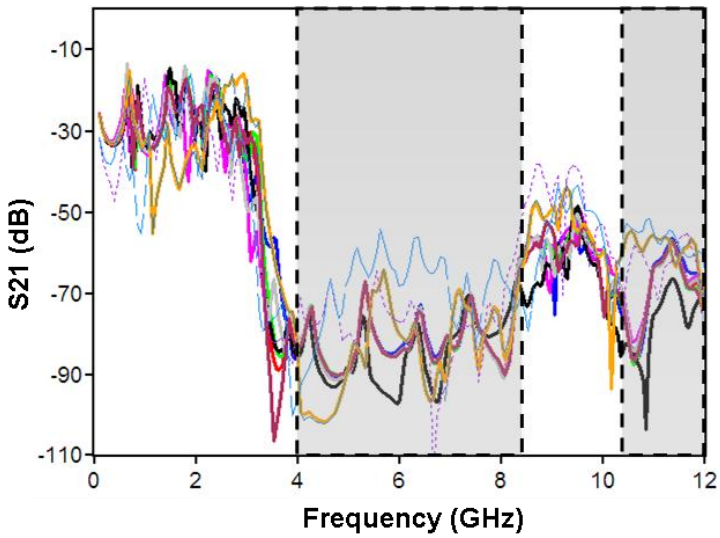


Figure 92 S21 (dB) plots for different port and aperture locations for structures in Figure 91 (Shaded areas correspond to isolation bands)

When the ports are located very close to the aperture, there is reduction in the isolation level across the ports. This is because the EBGs offer the band gap owing to perturbations induced in the propagating EM wave impedance by the alternating metal patches and branches forming the EBG structure. If the number of EBG cells between the excitation and response ports is reduced (i.e., happens if the ports are close to each other), the isolation level in the band gap reduces as the impedance perturbation experienced by the propagating wave is not very high.

The defect in the periodicity of the EBG structures caused by the presence of apertures results in defect modes which can occur within the EBG band gap. Figure 93 shows the S21 (dB) results for three different structures of lateral dimensions 25 X 25 mm, 42 X 42 mm and 59 X 59 mm with an aperture of size 6 X 6 mm. Aperture location is similar to Figure 91. Figure 94 shows the β-f plot obtained by incorporating the aperture in the unit cell similar to that shown in Figure 89b. The defect mode is circled in

Figure 93 and Figure 94 . Similarly, Figure 95 shows the simulated results for three different structures whose dimensions are 25 X 25 mm, 42 X 42 mm and 59 X 59 mm with an aperture size of 4 X 4 mm. Figure 96 shows the β-f plot obtained by including an aperture of 4 X 4 mm in the unit cell. Again in Figure 95 and Figure 96 the defect mode is circled in the plots. The effect of a slot or aperture is significant in the EBG cells which are immediately adjacent to it. Once the excitation and response points are shifted farther away, the effect reduces. For irregular shaped planes and for splits of varying widths across the planes, capturing the aperture coupling alone is not sufficient to convincingly describe the EM wave suppression behaviour.

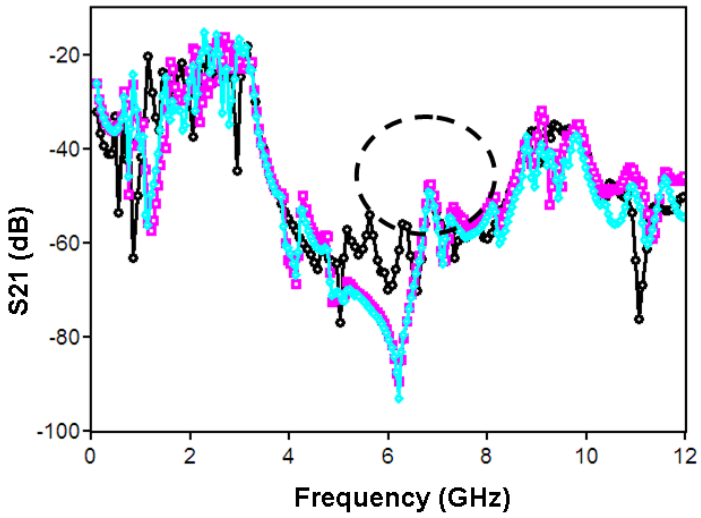


Figure 93 S21 (dB) response showing the occurrence of defect mode for aperture of size 6 X 6 mm

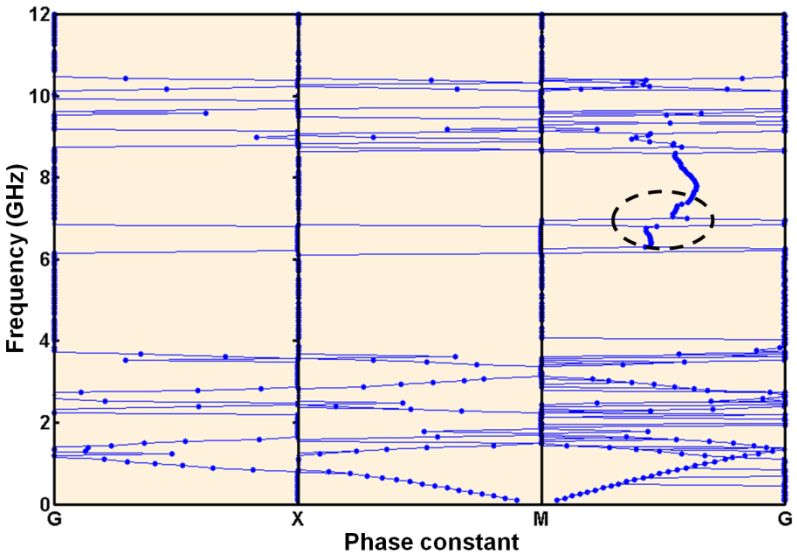


Figure 94 β–f plot showing the defect mode within the band gap region for the S21 parameters in Figure 93

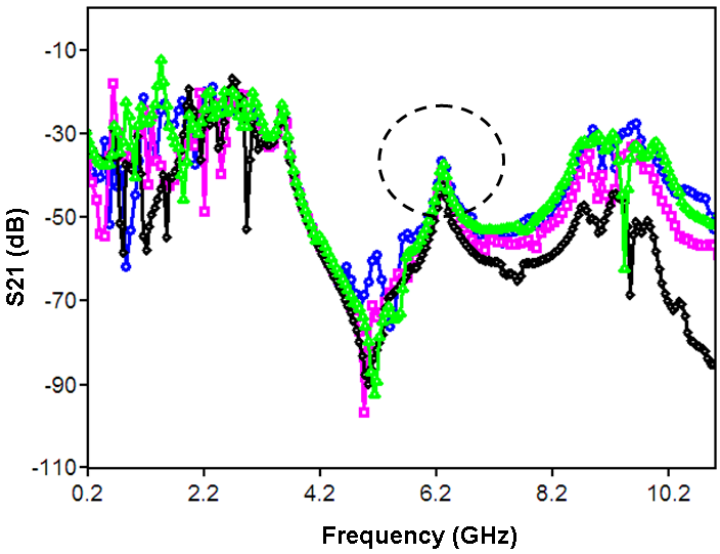


Figure 95 S21 (dB) response showing the occurrence of defect mode within the band gap for aperture of size 4 X 4 mm

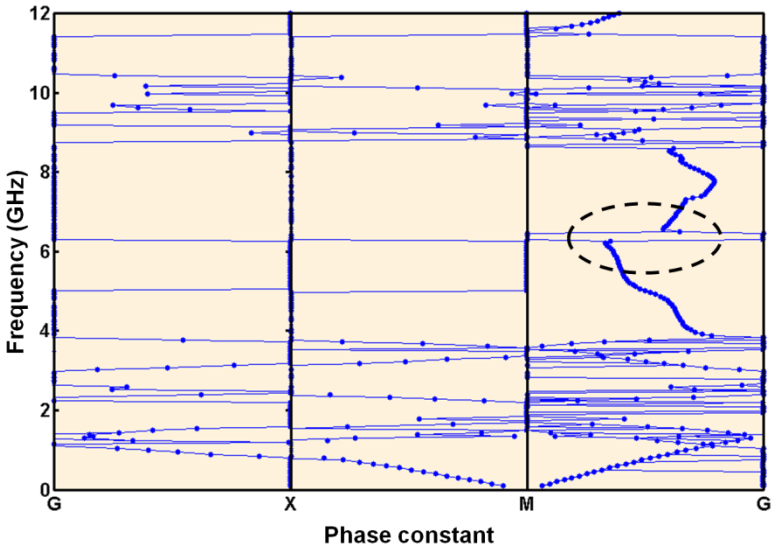


Figure 96 β–f plot showing the defect mode within the band gap region for the S21 parameters in Figure 95

4.2.1 Validation of Stop-Band Prediction by Measurements

To demonstrate the stop-band prediction methodology in multilayer packages, the predictions are validated against measurements from various multilayer structures. A test vehicle is fabricated as shown in Figure 97 to demonstrate this method on a substrate of size 26 X 35 mm. Figure 97 shows the 3D view of the fabricated test vehicle. EBGs were patterned on Plane 2 (center plane with aperture) of the structure in Figure 97. The size of each metal patch is 8 X 8 mm and each metal branch is 1 X 1 mm. Ports 1 and 2 are placed in bottom and top plane pair cavities as marked in the figure. It can be inferred from Figure 98 that the proposed technique suppresses vertical coupling into the GHz range. The beginning of the stop band is indicated by the negative slope in the graphs around 4GHz.

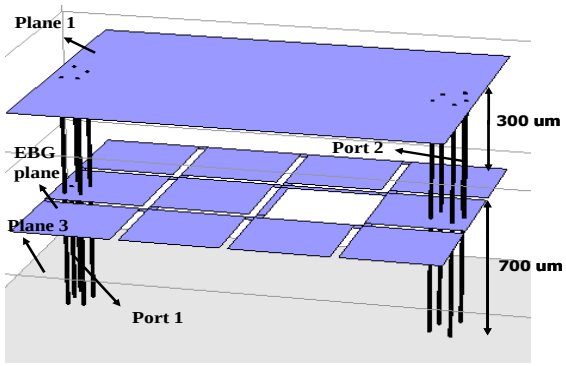


Figure 97 Three layer test vehicle

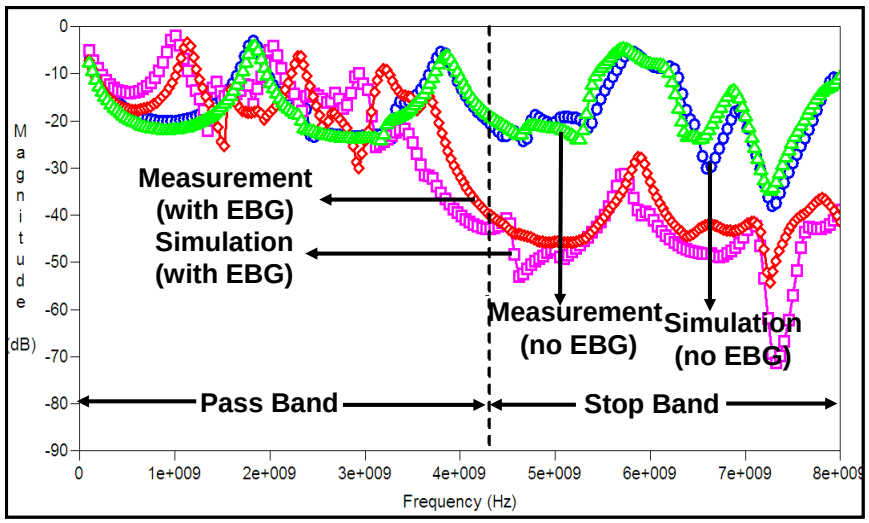


Figure 98 Comparison of Simulation and Measurement results for structure in Figure 97 with and without EBGs — S21 (dB) plots

A second set of test vehicles were fabricated consisting of larger sized multilayer substrates. Figure 99 shows the substrate stack-up for the fabricated test vehicles. Figure 100 shows the top view of the EBG plane (M2 layer) of a unit cell. Figure 100 shows four ports which are labeled — Ports 1–4. Port 1 and Port 2 are defined between M2–M3, while Port 3 and Port 4 are defined between M1–M2. Figure 101 shows the Phase Constant β vs. Frequency f plot with the regions where electromagnetic wave propagation is suppressed. Figure 102 shows two structures with different lateral

dimensions, namely 54 X 54 mm and 76 X 76 mm, with excitation and response ports in EBG cells which are adjacent to the aperture. Figure 103 compares the band gap obtained from the β−f plot with the S-parameter response measured from the structures in Figure 102. The areas, shaded in grey, in Figure 103, correspond to the stop band frequency regions. The defect mode due to the aperture is marked in Figure 101 and Figure 103. The circled region shows the peak in coupling within the band gap region.

Figure 99 Substrate stack-up used for Test Vehicle

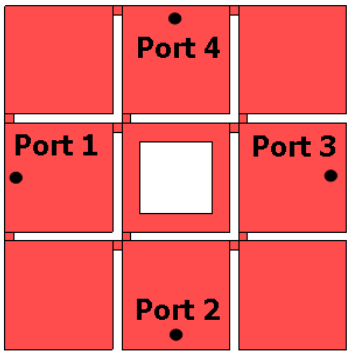


Figure 100 Top view of the M2 layer of unit cell used for the estimation of band gap regions

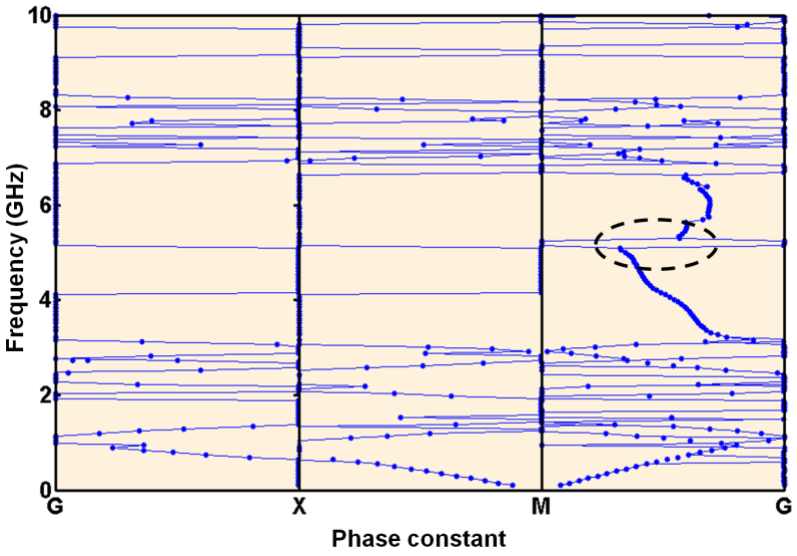


Figure 101 β–f plot showing the regions (shaded in gray) where suppression of vertical coupling is achieved, the circled area shows the occurrence of defect mode

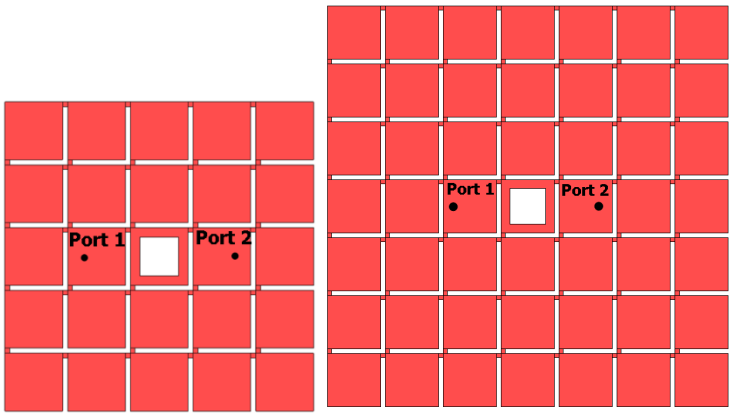


Figure 102 Top view of M2 layer for structures with ports located on cells adjacent to the aperture

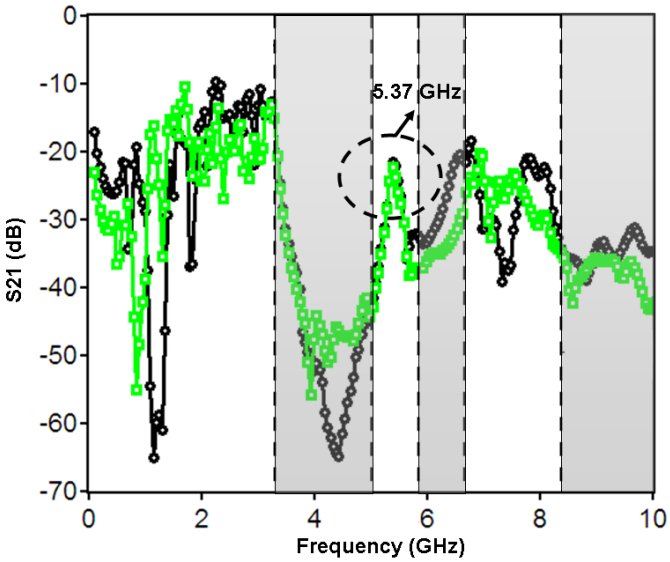


Figure 103 Comparison of predicted stop-bands with measured S-parameter results. The shaded areas indicate the frequency regions in which coupling suppression is achieved

Two structures with different lateral dimensions, 54 X 54 mm and 76 X 76 mm, and different port locations (case with ports not close to the aperture) are measured. Both structures have an aperture of 10 X 10 mm as shown in Figure 104. Figure 105 shows the unit cell simulated and Figure 106 shows the β–f plot. Figure 107 compares the S-parameter response obtained by directly measuring the structure with the predicted band gap from β–f plot. When the ports are very close to the aperture, regardless of the size of the aperture there is a reduction in the amount of isolation achieved, as the basis of EBG property is the impedance perturbation caused by the alternating patches and branches. Recall that if the number of cells between the excitation and response ports is reduced, the isolation level also reduces.

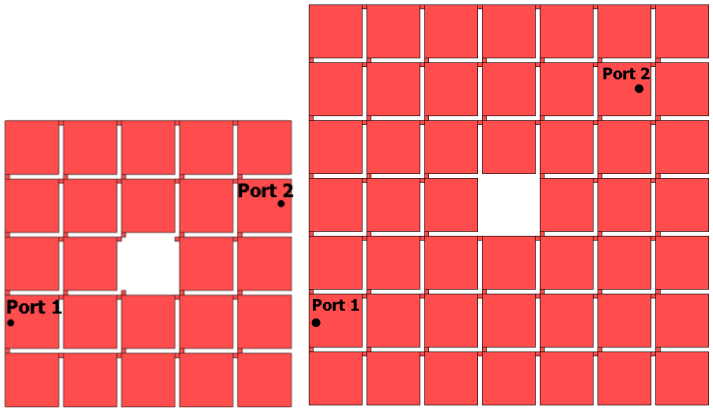


Figure 104 Top view of M2 layer for structures with ports located on cells which are not adjacent to the aperture

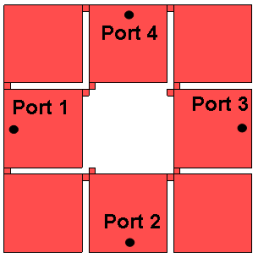


Figure 105 Top view of the M2 layer of unit cell used for the estimation of band gap regions

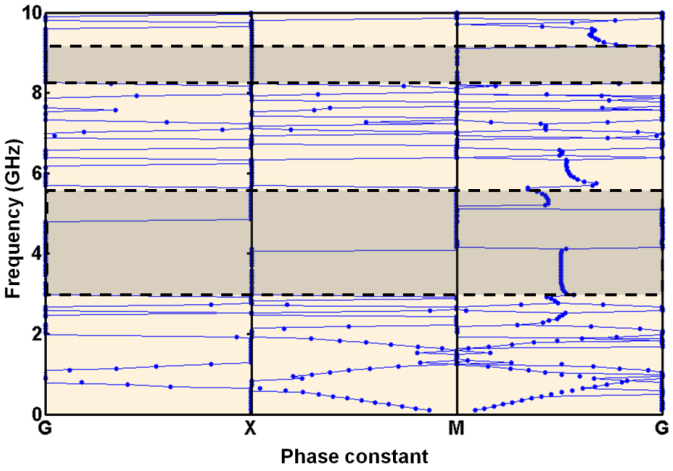


Figure 106 β–f plot showing the regions (shaded in gray) where suppression of vertical coupling is achieved

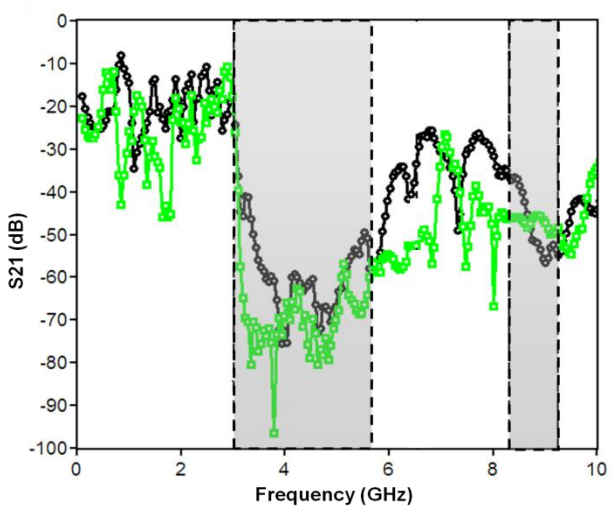


Figure 107 Comparison of predicted stop-bands with measured S-parameter results. The shaded areas indicate the frequency regions in which coupling suppression is achieved

4.3. Concluding Remarks

To conclude, this chapter presented a synthesis methodology for EBGs and subsequently a dispersion diagram based method for predicting the various pass bands and stop bands of the synthesized EBGs implemented for vertical coupling suppression in multilayer packages. The frequency range within which noise isolation is desired in a system forms the fundamental band gap of the EBG structures, and these are first synthesized using the band gap requirement. In the case of vertical isolation prediction, multiple plane pairs were involved and the periodicity of the EBGs was lost due to the presence of apertures/cutouts and ports at different plane pairs. To effectively predict the isolation in vertical direction, a 2D Dispersion diagram method was developed. In particular, the synthesized EBGs are analyzed using multilayer dispersion diagram method to accurately predict and validate the noise isolation performance in the

multilayer packages. The effectiveness of the proposed method in suppressing coupling has been validated using experimental simulations and measurement results.

CHAPTER 5

CHIP-PACKAGE INTERACTION IN PACKAGES WITH EMBEDDED CHIPS: ELECTROMAGNETIC COUPLING ON CHIP BOND PADS

Embedding chips within the package substrate results in packages that are thinner than those with surface mounted chips. However, this is true only if the packaging technology, in addition to embedding the chip, also makes use of the package area surrounding the chip for routing signal and power/ground supplies. In other words, the benefit of embedding the chip can be realized only if the metallization layers surrounding the chip are made functional. In chip-last method, the chip is embedded in flip-chip style to keep the parasitics of the chip to substrate interconnections as low as possible.

Figure 108 shows the layers surrounding the chip used for power and ground supplies, while Figure 109 shows the same layers being used for signal routing. In the figure, the power/ground layers are marked as P/G. Depending on the configuration of the system on the whole it may be appropriate to use the layers adjacent to the embedded chip either for power/ground supply, or for signal distribution as explained in Chapter 1. If the layers surrounding the chip are left unused, as in Figure 110, the package with embedded ICs may not provide significant advantages in terms of achieving smaller form factor over packages with surface mounted chips. This means that it is essential to study and analyze the interaction of the chip and package and the noise coupling effects they

have on each other under the configuration where the metal layers adjacent to the embedded chip are used for power delivery and signal distribution.

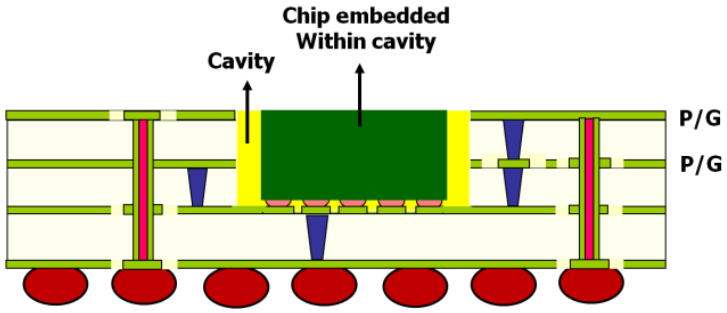


Figure 108 Layers surrounding the embedded chip are used as power-ground supply

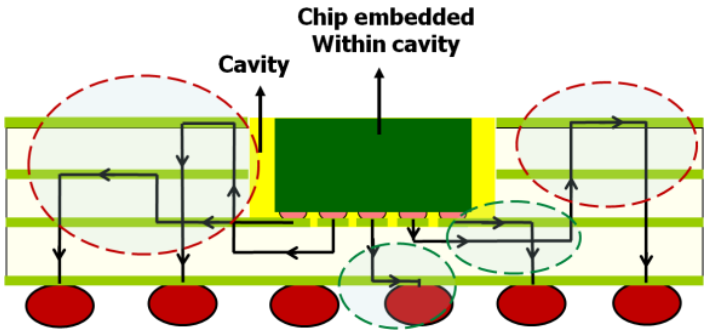


Figure 109 Layers surrounding the embedded chip are used for signal

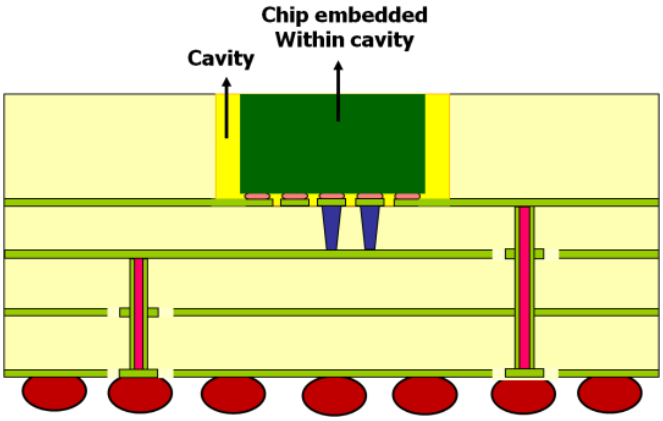


Figure 110 Surrounding metal layers not used in this configuration

In the following, prior work in chip-package interaction for packages with surface mounted chips is discussed. In packages with chips that are assembled using wire-bonds, the parasitics associated with the wire-bonds cause the internal voltages at the chip inputs to be different from the supply voltages [**73**]. The self parasitics contributed by the resistance and inductance of the bond wires cause ground bounce and VDD bounce on the voltages at the chip inputs. The mutual parasitics contributed by capacitive and inductive coupling across closely spaced bond wires result in electromagnetic coupling and crosstalk across wire-bonds of close proximity [**72**]. This drawback with wire-bond assembly can be overcome by using flip-chip assembly in which the chip to substrate interconnects are solder balls. These solder balls are attached to the bond pads on the package to form the interconnection between the chip and package. The parasitics (inductance and capacitance) associated with the solder bumps are much lower as compared to wire-bonds [**124**] [**125**] and hence they help in reducing voltage fluctuations experienced at the chip inputs. Flip-chip packages are effective even for millimeter wave packaging owing to the reduced interconnect parasitics and insertion and return losses associated with signal transmission through flip-chip interconnects [**126**].

Having discussed the chip to substrate interconnects in typical packages with surface mounted chips, the effects of electromagnetic coupling in the power distribution network of a package are discussed next. As explained in Chapter 1, the power distribution network in a package consists of multiple power and ground planes. The bond pads of the chip are routed through the package with transmission lines and vias. The power and ground pads of the chip are connected to the power and ground planes through via connections. The I/O signal bumps and their associated reference bumps are

routed through the package layers to the board with vias and trace lines. Any via transition through a parallel plate cavity formed by power and ground planes can result in EM wave radiation that propagates between the power and ground planes causing noise to couple with circuits powered by the planes. Signal integrity is affected when trace lines through the package change their reference planes, when signal vias cross through power–ground plane pair cavities, and due to noise coupling from the power distribution network (PDN) to the signal traces [**42**]. These are some of the commonly encountered challenges in preserving the signal and power integrity of packages with chips mounted on the package surface.

Chips embedded within the package experience greater influence from the package electromagnetic fields as compared to surface mount chips. When a chip is embedded within a multilayer substrate consisting of multiple power/ground planes, it is likely positioned either within a single plane pair cavity, or positioned such that it extends across multiple cavities. The transient currents in the vias that cross through parallel plate cavities formed by the power and ground planes in the package result in the propagation of electromagnetic waves through the PDN. As discussed in Chapter 2, the electromagnetic waves generated in the package couple vertically through apertures to adjacent plane pair cavities. When a die is embedded within a dielectric cavity formed in the substrate, it is prone to the interference of the electromagnetic waves. The noise that an embedded chip is exposed to, can affect the proper working of the chip. The difference in the embedded chip configuration as compared to the surface mounted chips is that the bond-pads of the embedded chip can be enclosed within the power-ground

plane pair cavities of the package wherein the electromagnetic coupling from the package directly attacks the bond pads of the embedded chip.

Figure 111 shows a configuration of a chip embedded within a package that consists of power/ground planes in its PDN. This chapter analyzes and demonstrates the effects of package power/ground plane excitations on the bond pads of the chip embedded within the dielectric cavity. The blue arrow in the figure below represents a via transitioning through the bottom plane pair cavity.

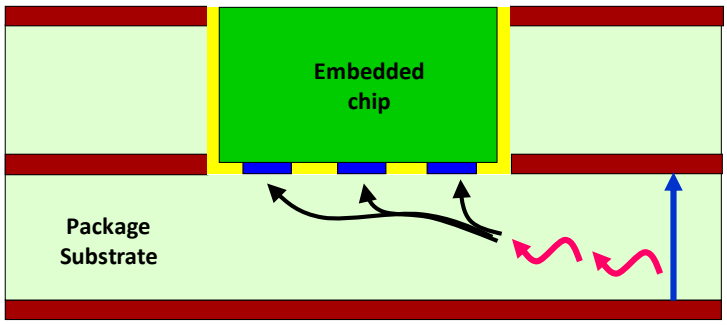


Figure 111 Cross-section of a package with embedded chip showing EM coupling to the die bond-pads

5.1. Coupling to the die bond-pads

In this section, the effect of excitation on the bond pads of an embedded chip for the case where the embedded chip does not require any back metallization is studied. Consider a multilayer stack-up as shown in Figure 112, which consists of three power/signal/ground metal layers, labeled as M1, M2 and M3. In Figure 113, the top view of the package shows the aperture on plane M1 and the bond pads of the embedded chip on layer M2. In this setup, it is of interest to study the coupling experienced by the

bond pads of the embedded chip (P3a and P3b) due to the excitations in the package (P1). These excitations usually happen due to current sources that are setup when vias that carry transient currents or signals transition through the power – ground parallel plate cavity. These vias radiate EM waves and the plane pair cavity formed by the power and ground plane acts as a parallel plate wave guide transmitting the generated EM waves. Now, if the bond pads are contained within such a plane pair cavity formed by the power and ground planes, they will experience substantial amounts of coupling due to the EM waves propagating in the plane pair cavity. Such a situation is common in the case of embedded chips, which is the reason why it is important to study this effect. The substrate bond-pads have a metallurgical connection with the die contact pads, which means that the parasitic coupling can affect the voltage at the inputs of the chip. The variations in the internal supply voltages can lead to logic errors, thus affecting the normal functioning of the chip. This section analyzes the effect of electromagnetic coupling to the bond pads of the chip.

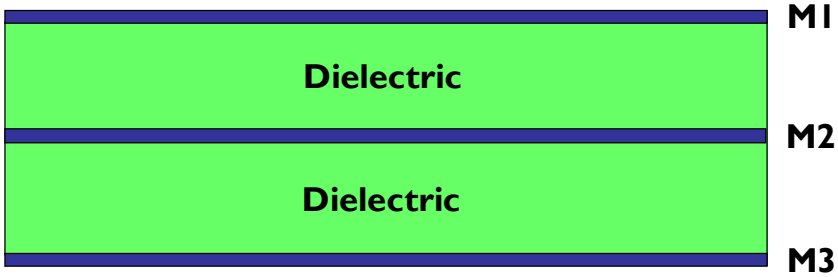


Figure 112 Multilayer package stack-up

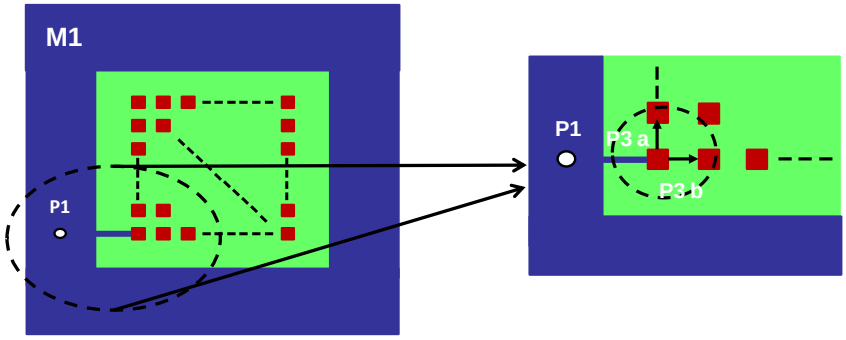


Figure 113 Top view of the multilayer structure showing the power/ground plane aperture and embedded bond pads

Figure 114 shows examples of array area and peripheral bond-pad layouts for chips [**127**]. The red, black and blue pads are power, ground and signal, respectively. Figure 115 shows the design rules for bump spacing from die boundary for both peripheral and array area bond-pad layout [**128**]. As an example, if the pitch is 200 um, considering a chip with peripheral pad layout, the distance of the pad from the die edge can get down to 200 um. Considering a clearance of 100 um between the die edge and cavity wall, the chip bond-pad can get to a distance of about 300 um with the edge of apertures made on power and ground planes for embedding the chip. This distance is marked as "A" in Figure 116. Also, assuming a reasonble value for the distance "X" (shown in Figure 116b) as 1 mm – 1.5 mm, the total distance between an excitation location (Port1) and response location (Port 2) can be around 1.5 - 2 mm approximately. In the test cases analyzed in this section, this spacing is assumed to be 2.5 – 4 mm. The proximity of the bond-pad to the aperture edge influences the coupling from the package to the bond-pads. This is because the fields fringing from the edges of the apertures (on power and ground planes) on to the bond-pads of the embedded chip get more and more significant with increasing proximity.

In this section, several cases with different power/ground plane arrangements have been simulated and the results have been validated with test vehicles fabricated on a six layer stack-up shown in Figure 117. The stack-up consists of six metal layers named M1 through M6. The dielectric material used is RXP developed by Rogers Corporation. The stack-up is made up of a core layer with dielectric material RXP1 between metal layers M3 and M4. The loss tangent of this material is 0.0038, the dielectric constant is 3.39 and the thickness of the core is 0.1 mm. This core has build-up layers on either side made up of the dielectric material, RXP4, with a loss tangent of 0.0043 and dielectric constant of 3.01. There are two build-up layers on top of the core of thicknesses 0.055 mm between M1 and M2, and 0.022 mm between M2 and M3. A similar build-up layer configuration is present at the bottom side of the core as well. Additionally, the build-up layer between M1 and M2 has a cavity for embedding the chip. The rationale behind designing a multilayer stack-up is to build a versatile test vehicle, where different layers can be assigned as power and ground, and the impact of EM coupling on the bond pads can be studied for these various cases. Note that the bond pads of the embedded chip are present on M2 layer. The cases discussed below have various configurations of power and ground planes assignments to the different layers in this test vehicle. The test vehicle consists of multiple coupons of sizes 14 X 14 mm and 10 X 10 mm with a cavity size of 4 X 4 mm for embedding the chip. A gap of 100 um is provided between the cavity and the plane edge on all four sides of the cavity to facilitate chip assembly. The following cases are analyzed through simulations and measurements to demonstrate the effect of electromagnetic coupling on the chip bond-pads.

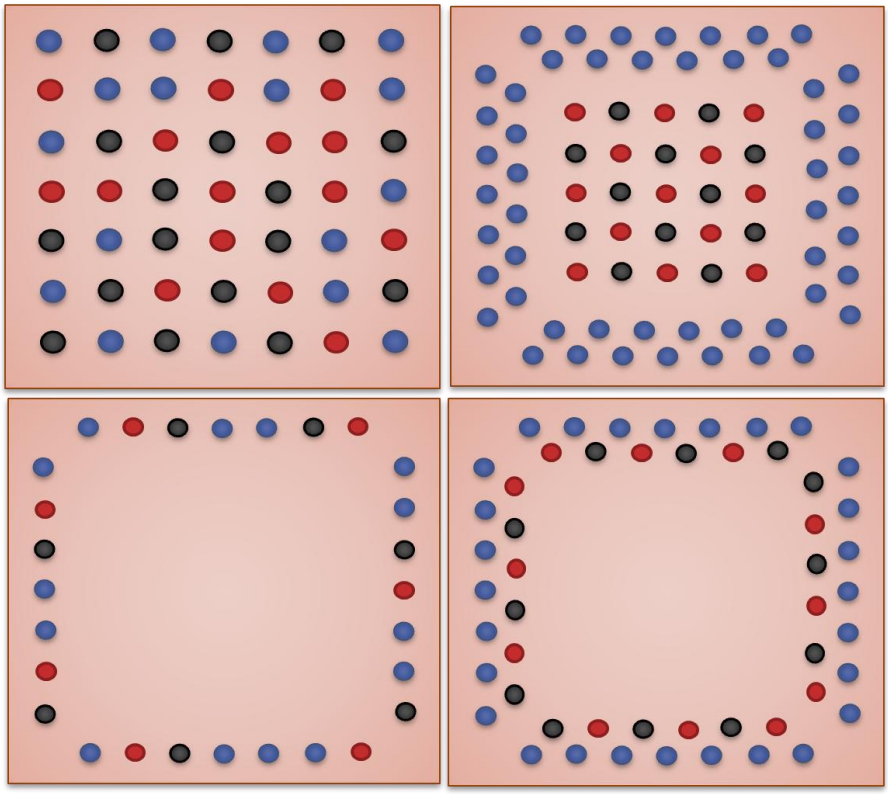


Figure 114 Array area (top row) and peripheral (bottom row) chip bond pad layouts

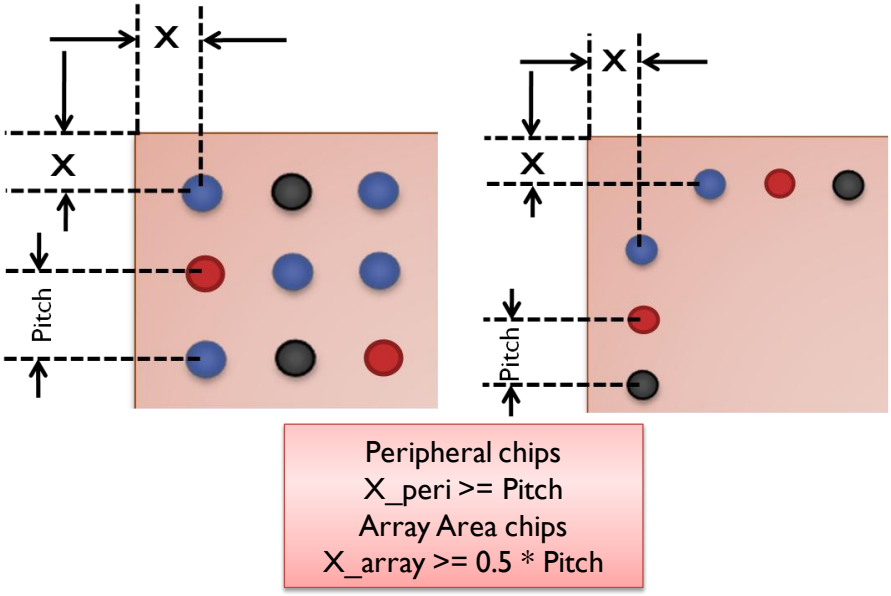


Figure 115 Design rules for bump spacing from die edge in chips with array area and peripheral bond pad layouts

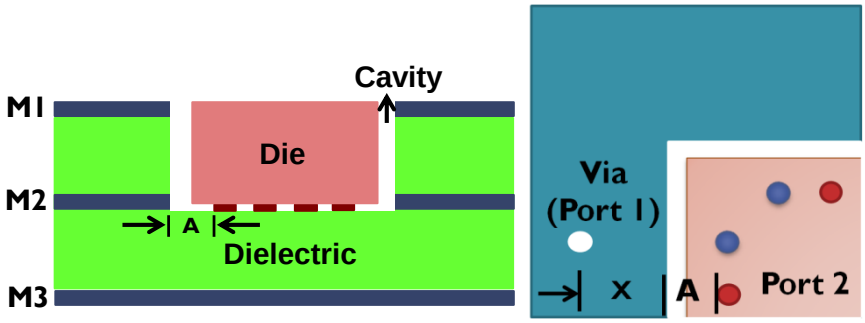


Figure 116 a) Cross-section of package with embedded chip, b) Top - view of a) showing bond pad and via spacing

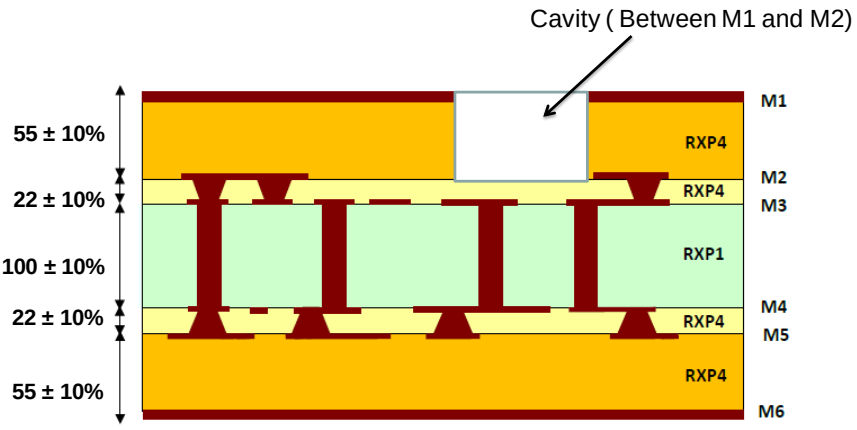


Figure 117 Six layer package for embedding chip

5.2. Case 1a: M3 as power and M2 as reference

In this configuration, planes M1 and M2 have an aperture corresponding to the region where the die is to be embedded and plane M3 forms a solid reference. The size of the package is 14 X 14 mm and the cavity is 4 X 4 mm. In addition, M2 layer also consists of the substrate bond-pads of the embedded chip. The cross-sectional view of this configuration is shown in Figure 118 and a schematic of the layout is shown in Figure 119. Figure 120 shows the simulation model from the EM Solver CST. The simulation model consists of layers M1 through M3. Since the contact pads of the chip

have a direct metallurgical connection with the substrate bond-pads, it is approximated as a single pad in the simulations. In Figure 118, P1 indicates an excitation on the package (measured between planes M3 and M2) and P3 is a response point to measure the coupling on a bond pad (between bond pad on M2 and M2 plane). P2 is similar to P1, defined across M3 and M2, but is not shown in Figure 118. This is to measure the resonances in the plane pair cavity formed by the planes in layers M3 and M2. Figure 121 is a picture of the fabricated test vehicle. The probe pads on the M1 plane and the embedded bond pads were probed directly using Air Coplanar probes of GSG configuration with a pitch of 500 um. The distance of the bond pad from the cavity wall is 0.5 mm and from the probe pads on the plane M1 is 2.5 mm. Figure 122 shows the comparison between simulated and measured S and Z parameters, respectively. The plots show the variation of S and Z parameters with respect to the frequency in GHz, where the highlighted regions show the correlation between the peaks in the coupling observed at the bond pads and the power plane resonances. As seen from the graph there is a high level of coupling, reaching a maximum of over -30 dB at frequencies corresponding to the occurrence of power plane resonances, which are highlighted in Figure 122.

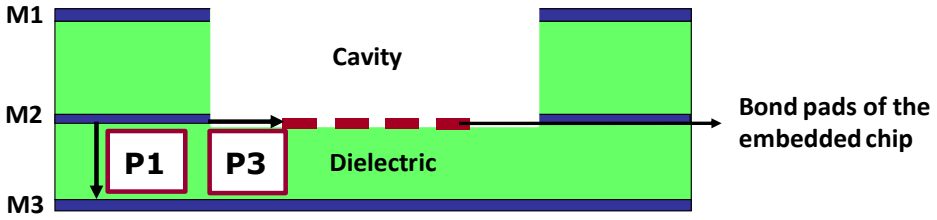


Figure 118 M3 as power and M2 as reference

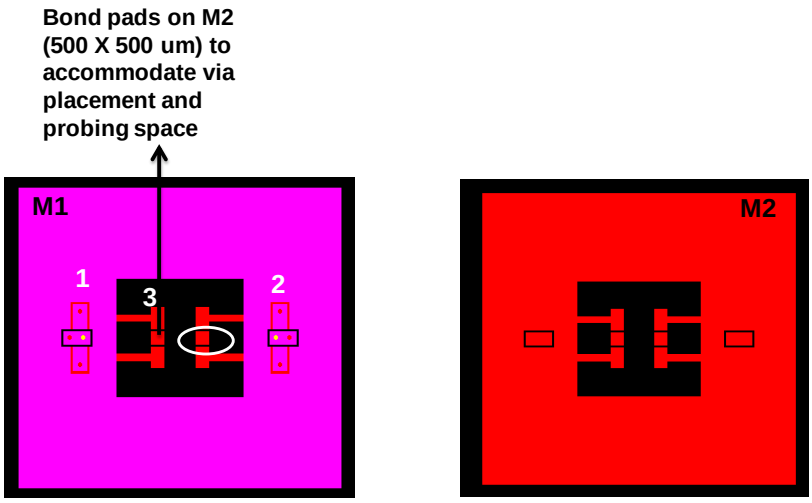


Figure 119 Layout of Case 1 coupon showing the top views of layers M1 and M2

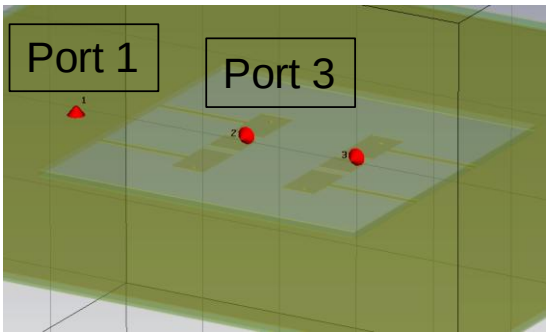


Figure 120 Simulation model from 3D EM Solver (CST)

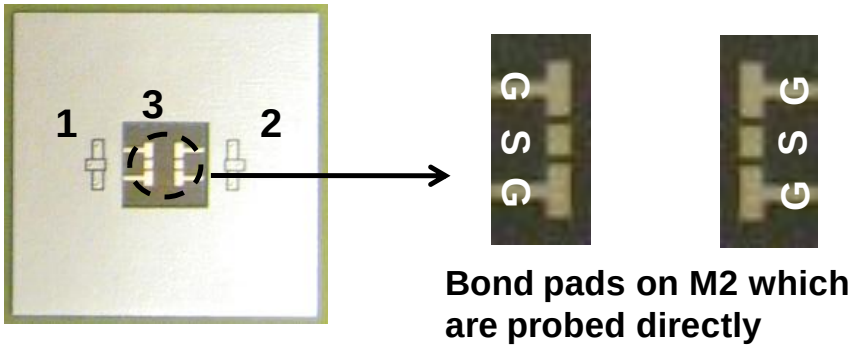


Figure 121 Picture of test vehicle coupon

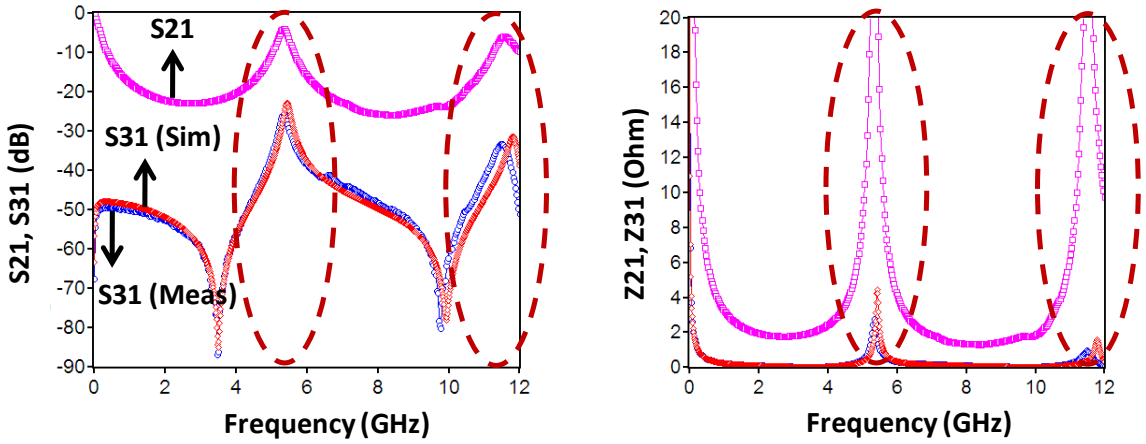


Figure 122 S and Z parameters showing the power plane resonance and bond pad coupling results from simulations and measurements

5.3. Case 1b: M3 as power and M2 as reference

This case is similar to Case 1a, but here the point of probing between M2 and M3 is moved farther from the location of the bond pads. The distance in Case 1a was 2.5 mm; here it is increased to 4 mm. In Figure 123, the S parameter plot shows the coupling between P1 (across planes M2–M3) and P2 (at the bond pad). Figure 124 shows the corresponding Z parameter plots, thereby validating the simulation result from the EM solver, CST, and the measurement result. In this configuration, this change does not cause any considerable variations in the level of coupling observed at the resonant frequency as compared to Case 1a. This is because the signal pad and power plane on layer M3, which are both excited with respect to M2, are retained at the same locations with respect to each other in spite of the probing point on the plane being moved farther away.

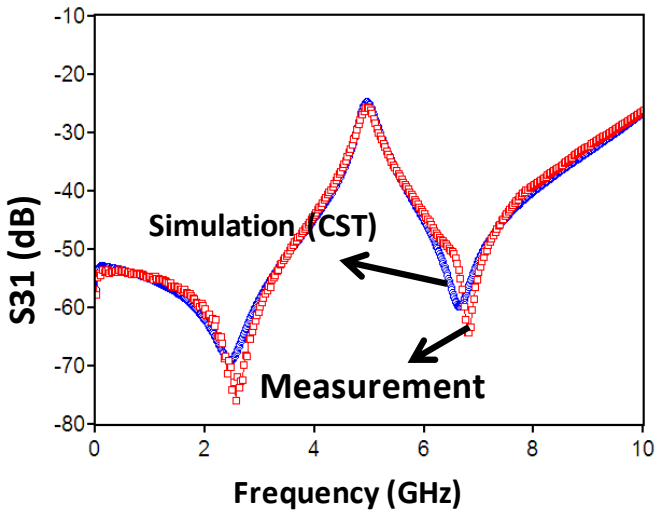


Figure 123 S-Parameter — Coupling between package excitation (Port 1) and embedded bond pad (Port 3)

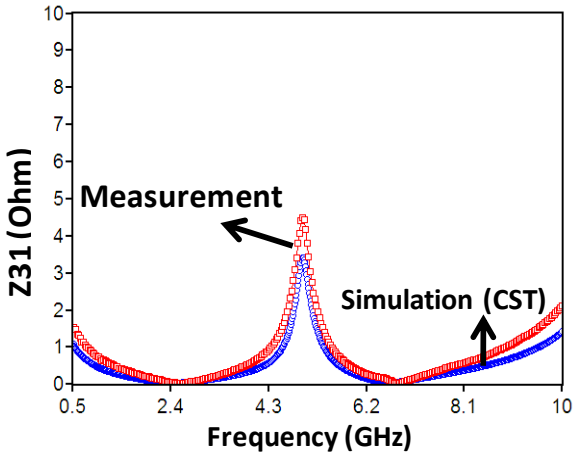


Figure 124 Z-Parameter — Coupling between package excitation (Port 1) and embedded bond pad (Port 3)

5.4. Case 1c: M3 as power and M2 as reference

This is similar to Case 1b but the package size at 10 X 10 mm is smaller as compared to the previous case where the package size was 14 X 14 mm. Figure 125 shows a picture of multiple coupons from the test vehicle where Case 1c is highlighted.

Figure 126 and Figure 127 show the comparison between the simulated and the measured S and Z parameters, respectively. The plots show the variation of S and Z parameters with respect to the frequency in GHz. As seen from the graph there is a high level of coupling, reaching a maximum of over -20 dB around 6.4 GHz, to the die bond-pads due to the excitation across the package planes. The frequency of maximum coupling is pushed higher as compared to Case 1b due to the smaller size of the package.

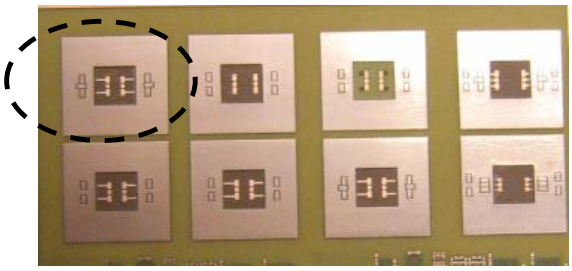


Figure 125 Picture of test vehicle coupon

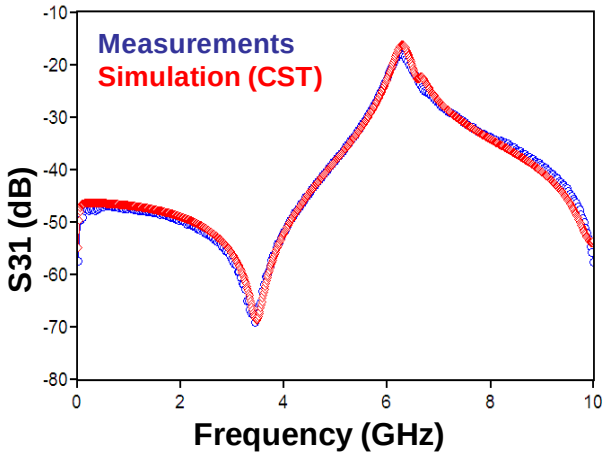


Figure 126 S-Parameter — Coupling between package excitation (Port 1) and embedded bond pad (Port 3)

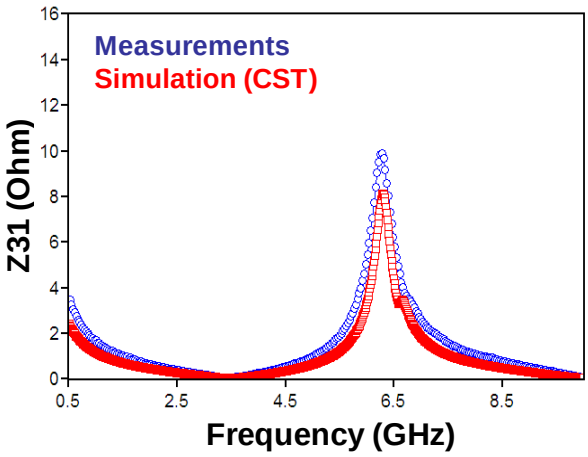


Figure 127 Z-Parameter — Coupling between package excitation (Port 1) and embedded bond pad (Port 3)

5.5. Case 2: M1 as power and M2 as reference

In this configuration, planes M1 and M2 have an aperture corresponding to the region where the die is to be embedded and plane M3 is a solid reference. The size of the package is 14 X 14 mm and the cavity is 4 X 4 mm. In addition, M2 layer also consists of the substrate bond-pads of the embedded chip. The cross-sectional view of this configuration is shown in Figure 128, and Figure 129 shows the top view of M1 and M2 layers. This case is similar to Case 1 except that the power-ground plane pair combination is changed. In this case, both the power and ground planes have apertures of the same size. Here, again the frequencies at which the parallel plate cavity resonates, gives rise to maximum coupling to the bond pads. In Figure 129, P1 indicates an excitation on the package (measured between M2 and M1) and P3 is a response point to measure the coupling on a bond pad (between bond pad on M2 and M2 plane). P2 is similar to P1, assigned across M1 and M2, and is used to measure S21 parameter. In

Figure 130, the S parameter plots for S21 (dB) and S31 (dB) are shown. As seen from the plots, the peaks in S21 and S31 match. In this case, the low frequency coupling is low and it increases with frequency. The fields fringing from the edge of the aperture on M1 couple with the bond pad on M2 and this causes the resonances in S31. This coupling due to the fringe fields across the aperture edge on M1 plane and the bond pad on M2 is small at low frequencies and it increases with frequency. This is similar to the behavior of coupling across gaps and slits.

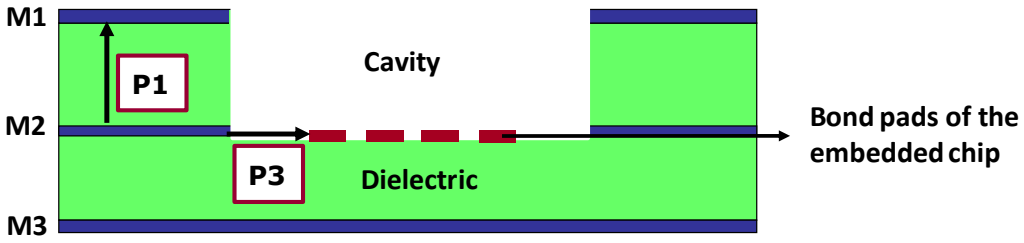


Figure 128 M2 as reference (Ground), M1 as Power

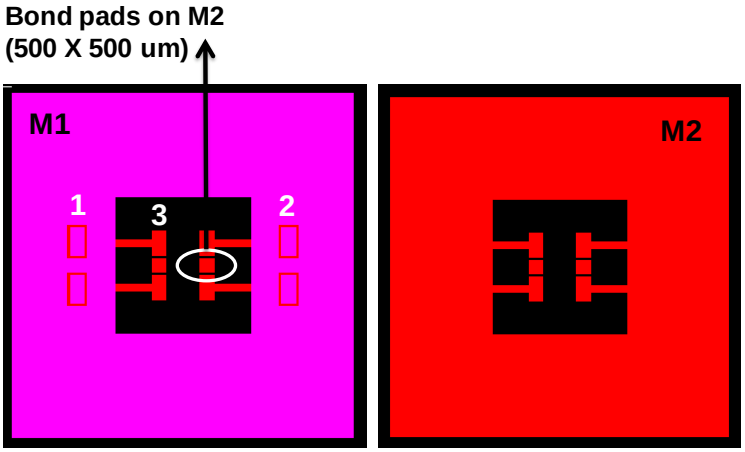


Figure 129 Top view of Case 2 coupon showing the M1 and M2 layers

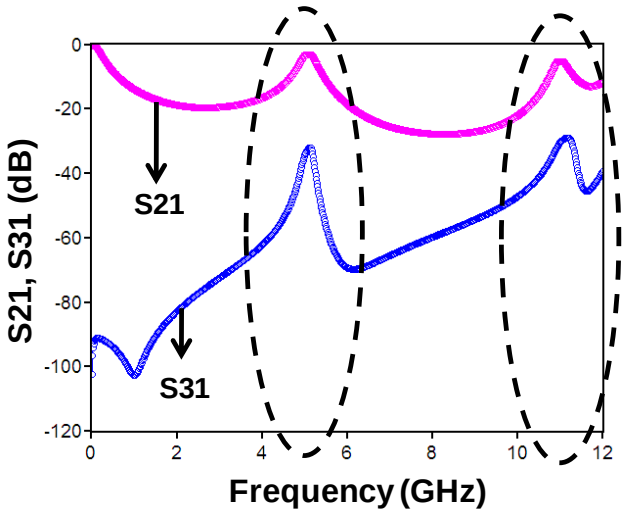


Figure 130 S-Parameter response for power-ground cavity resonance between Ports 1 and 2 (S21) and bond pad coupling between Ports 1 and 3 (S31)

5.6. Case 3: M1 as Power and M4 as Ground

In this configuration, plane M1 has an aperture corresponding to the region where the die is to be embedded and plane M4 is a solid reference. Plane M2 consists of the bond pads of the chip. This case is distinguished from Cases 1 and 2 in the sense that there is no plane on M2, which supports the bond pads. This case is of more significance from a practical standpoint since the metal layer, which supports the substrate bond pads, is entirely used for fan-out of the chip bumps. Two variations in the package size were considered, which were 14 X 14 mm and 10 X 10 mm, while the cavity size remained the same at 4 X 4 mm for both the cases. The cross-sectional view of this configuration is shown in Figure 131 and a schematic of the layout is shown in Figure 132. Figure 133 shows the simulation model from the EM Solver CST. The simulation model consists of layers M1 through M4. As before, the contact pads of the chip are approximated as a single pad in the simulations. In Figure 131, P1 indicates an excitation on the package

(measured between M1 plane and M4 plane) and P3 is a response point to measure the coupling on a bond pad (between bond pad on M2 and M4 plane). P3 is at a distance of 0.5 mm from the edge of the 4 X 4 mm aperture made on the planes and the distance between P1 and P3 is 2.5 mm. In Figure 133, P3a and P3b indicate two response points on each of the bond pads used in the simulation. Figure 134 is a picture of the fabricated test vehicle showing the embedded bond pads probed directly using Air Coplanar Probes (ACP) of GSG configuration and a pitch of 500 um. Figure 135 and Figure 136 show the comparison between the simulated and the measured S parameters for package sizes 14 X 14 mm and 10 X 10 mm, respectively. The plots show the variation of S parameters with respect to the frequency in GHz. These S parameters are measured between P1 and P3a. As seen from the graph the coupling reaches a maximum of about -40 dB, for the 14 X 14 mm package and over -50 dB for the 10 X 10 mm package. Similar to the previous cases, the coupling to the bond pad reaches a maximum at the frequencies of power plane resonances. In this test vehicle, the total thickness of the core and buildup layers comes to 0.177 mm. As the thicknesses of the materials increase, the magnitude of bond pad coupling increases to higher levels as will be demonstrated later in this chapter.

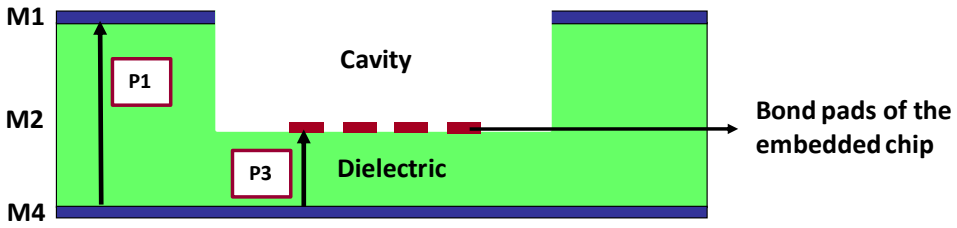


Figure 131 M1 as power and M4 as reference

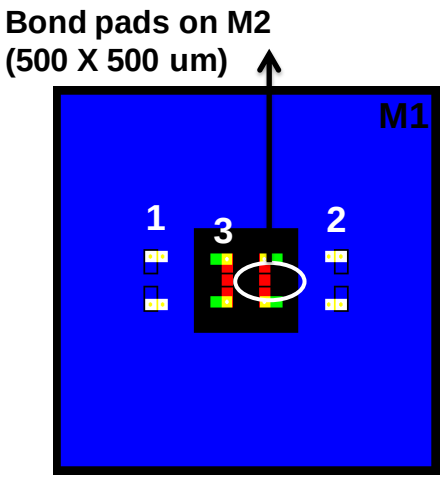


Figure 132 Top view of layout showing the aperture on M1 and bond pads on M2

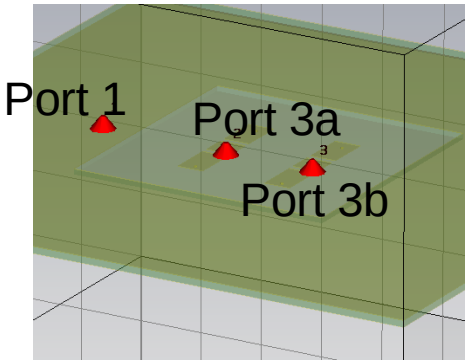


Figure 133 Simulation model from 3D EM Solver (CST)

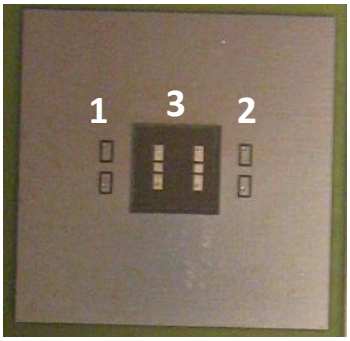


Figure 134 Picture of test vehicle coupon

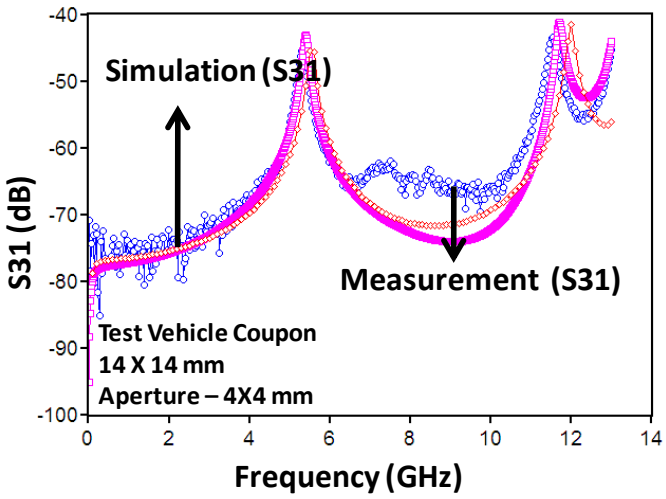


Figure 135 S-Parameter — Coupling between package excitation (Port 1) and embedded bond pad (Port 3) for test vehicle coupon of size 14 X 14 mm

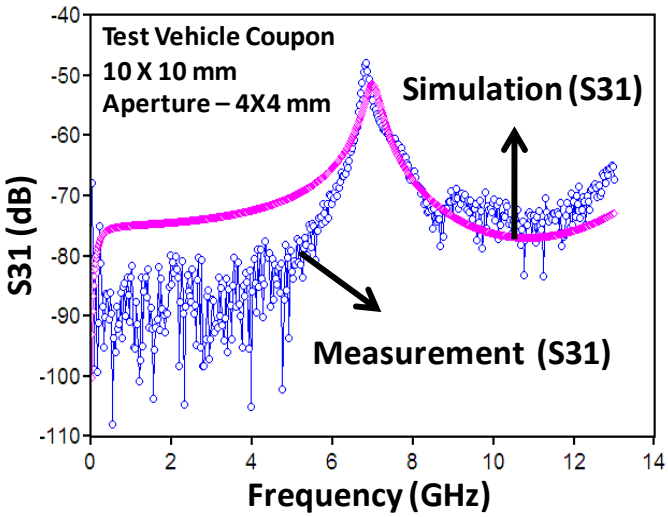


Figure 136 S-Parameter — Coupling between package excitation (Port 1) and embedded bond pad (Port 3) for test vehicle coupon of size 10 X 10 mm

5.7. Noise Voltage at the Bond Pads

In this section, the effect of EM coupling to the bond pads is discussed in terms of noise voltage. In the previous section, the impact of EM coupling was studied in the

frequency domain, while here the voltage fluctuations that arise due to the EM coupling are studied in the time domain. So far in this chapter, it has been shown through different cases as to how the EM waves setup in the plane pair cavities, whenever there are via transitions across the power ground planes, couple with the bond pads of the embedded chip. Voltage fluctuations are caused at various locations on power planes due to EM coupling and this phenomenon is also observed at the bond pads whenever the excitations on the power planes couple significantly to the bond pads. The voltage fluctuations measured with respect to time provide an idea of the duration for which the bond pad voltages oscillate. This means that the internal circuitry of the chip connected to the bond pads undergoes voltage fluctuations. The chip experiences voltages that are different from the steady state high and low values. If the noise voltage margin is very small, the voltage fluctuations which are transferred to the internal circuitry can result in malfunctioning of the chip. This makes it important to understand the phenomenon of voltage fluctuations impacting the bond pads in order to effectively minimize the effect of coupling from the package.

Case 3 from the previous section, is chosen for noise voltage analysis. Since case 3 is the most commonly encountered configuration in any multilayer package, it is further analyzed in the time domain as well. Recall that in Case 3, a separate metallization layer is exclusively assigned for the fan out of chip bond pads. In the following, time domain simulation methodology is discussed.

The multiport S-parameter block obtained from frequency domain simulations, which was used to quantify EM coupling on the dB scale in the previous section, is converted into a broadband spice model. This model is analyzed through a transient

simulation performed using the circuit simulator tool from Agilent Technologies, ADS. Figure 137 shows the simulation setup in the 3D EM solver CST. M1 plane with the aperture to accommodate the die is assigned as power and M4 plane which is completely solid is the ground reference. The chip bond pads are present on the M2 layer. The package size is the same as that in Case 3, which is 14 X 14 mm. This structure is simulated with four different ports. Port 1 is the location of excitation across the plane pair M1–M4, corresponding to the location from which a chip driver draws current from the package PDN while switching. Port 2 is assigned at the bond pad on M2 with respect to the M4 ground plane. Port 3 is across the planes M1 and M4 which corresponds to the point where external power supply is connected to power up the package PDN. Port 4 is similarly across M1–M4 planes, which serves as the observation point to monitor the voltage fluctuation on the package PDN when Port 1 is excited. This structure is simulated in frequency domain and the 4-port S parameter block is obtained from CST.

Figure 138 shows the model for time domain simulations. The S-parameter block obtained from CST is converted into a broad band spice model with 5 ports using ADS. Port 1 is the excitation on the power plane which corresponds to the location where a current pulse is initiated. The current pulse shown in Figure 139, is modeled as a triangular PWL source operating for one cycle with the peak value of current reached being 10 mA. The rise time of the pulse is 50 ps and the fall time is 150 ps. Port 2 is assigned on the bond pads and this port terminal is assigned a variable V2 for monitoring the voltage fluctuation. A voltage supply of 3.3 V, which is commonly used in portable and desktop systems, is applied at Port 3. Port 4 terminal is assigned a variable, V4, for monitoring the voltage fluctuation on the package power-ground plane pair due to the

current pulse at Port 1. Port 5 is an additional port in the time domain, which was not present in frequency domain, used to create an absolute ground reference. V2 and V4 are the two quantities that are plotted with respect to time to demonstrate the voltage fluctuation on the package planes and the bond pads whenever there is any excitation on the power/ground planes in the package PDN. The variations in V2 and V4 over time indicate the intensity of voltage fluctuations that are induced. A transient simulation, as shown in Figure 138, for the duration of 50 ns with a 100 ps time step is performed.

Figure 140 shows the coupling between Port 1 across planes M1–M4 and Port 2, which is at the bond pad on M2 for three different cases as listed below. The dielectric material used is FR–4 with a dielectric constant of 4.5 and a loss tangent of 0.01

1. Dielectric thickness between M1 and M4 layers — 200 um
   Spacing between Port 1 (current pulse) and Port 2 (bond pad) — 1 mm
   Bond pads are located on M2 layer inside a cavity of thickness (between M1 and M2 layers) — 60 um
2. Dielectric thickness between M1 and M4 layers — 200 um
   Spacing between Port 1 (current pulse) and Port 2 (bond pad) — 2.6 mm
   Bond pads are located on M2 layer inside a cavity of thickness (between M1 and M2 layers) — 60 um
3. Dielectric thickness between M1 and M4 layers — 100 um
   Spacing between Port 1 (current pulse) and Port 2 (bond pad) — 1 mm
   Bond pads are located on M2 layer inside a cavity of thickness (between M1 and M2 layers) — 60 um

As seen from the results plotted in Figure 140 (where the three plots marked 1, 2 and 3 correspond to the three cases listed above, respectively), the coupling to the bond pads depends on the dielectric thickness of the material used between the power – ground planes, and the bond pad and its reference ground plane. It also depends on the distance of the cavity edge on the power - ground planes and the bond pad location. As the dielectric material gets thicker (200 um vs. 100 um), the coupling increases with the port locations maintained the same and as the proximity of the aperture edge on the planes and the bond pad increases, the coupling increases with the dielectric thickness kept constant, which is 200 um in this case. In cases 1 and 2, Port 1 is maintained at the same distance of 0.5 mm from the plane edge and bond pad location (Port 2) is varied to change the distance between Ports 1 and 2 from 1 mm to 2.6 mm.

The noise voltage or in other words the voltage fluctuation observed at the bond pads for the three different conditions analyzed here as 1, 2 and 3 are shown in Figure 141, Figure 142 and Figure 143 along with the respective voltage fluctuation on the power planes (V4). The maximum voltage fluctuation is observed for the first case where the total dielectric thickness of the package is 200 um and the proximity between Ports 1 and 2 is 1 mm. The corresponding fluctuation on the planes M1–M4 at Port 4 due to the excitation at Port 1 is about 80 mV. In the second case, the dielectric thickness is maintained at 200 um and the proximity of Ports 1 and 2 is made farther from 1 mm to 2.6 mm. The fluctuation on the plane remains the same around 80mv but that observed at the bond pad is reduced to a maximum of 11.4 mV from 39 mV as was in the first case. In the third case, when the dielectric thickness is reduced to 100 um for the same port

locations as in the first case, the fluctuation at Port 4 comes down to about 40 mV and the fluctuation on the bond pad is reduced to less than 7 mV.

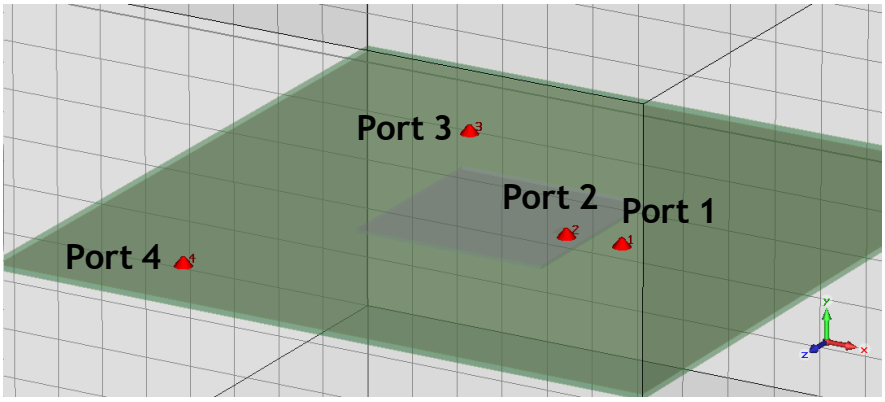


Figure 137 Simulation model from 3D EM Solver (CST)

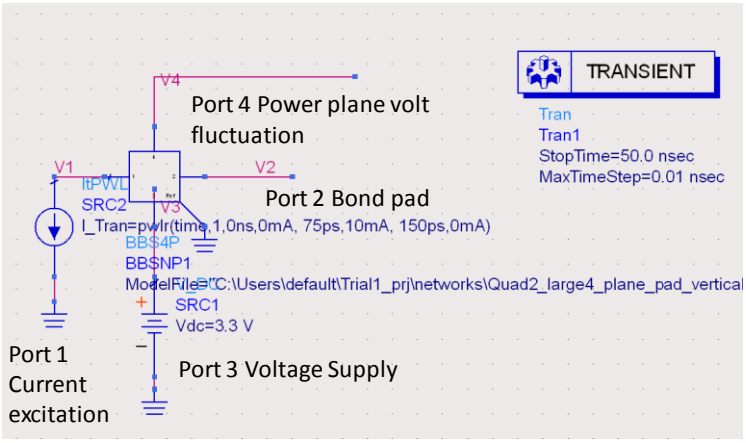


Figure 138 Circuit simulation model for computation of voltage fluctuation in time domain

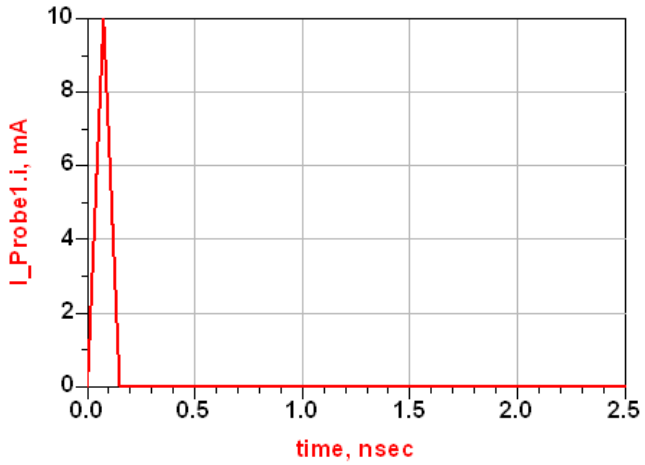


Figure 139 Triangular current pulse for exciting the multilayer PDN

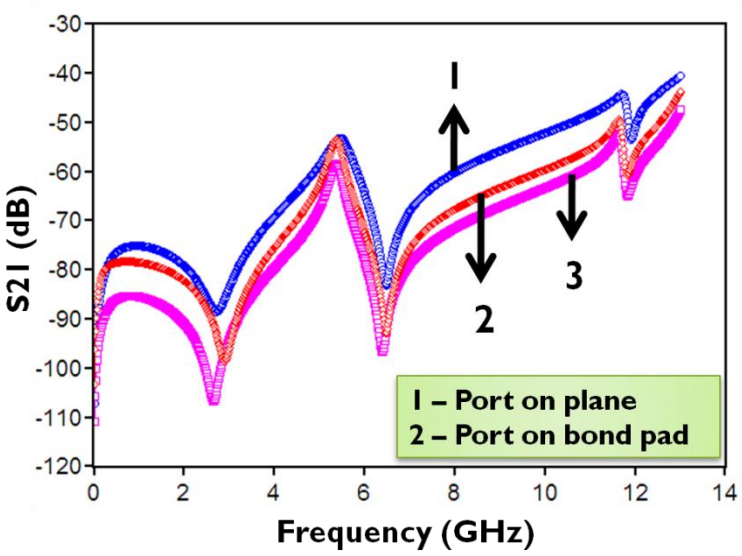


Figure 140 Coupling to the bond pads

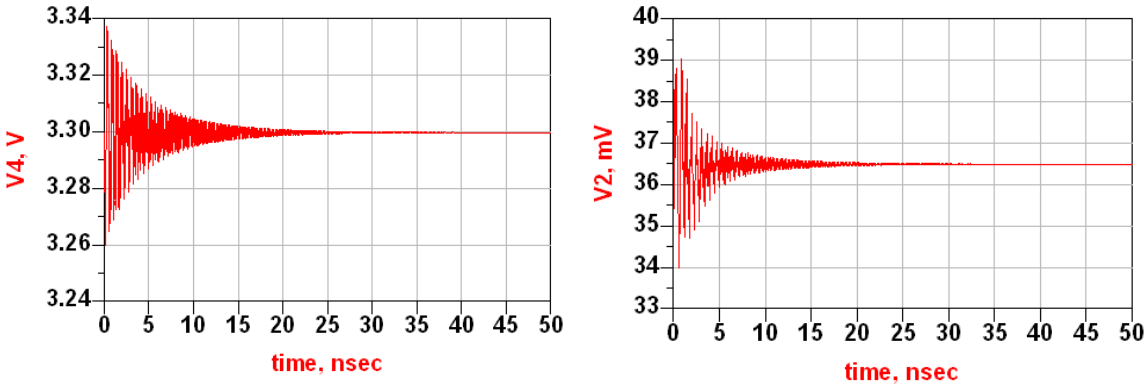


Figure 141 Voltage fluctuations at Port 4 (V4) in left, and at Port 2 (V2) in right for Case 1

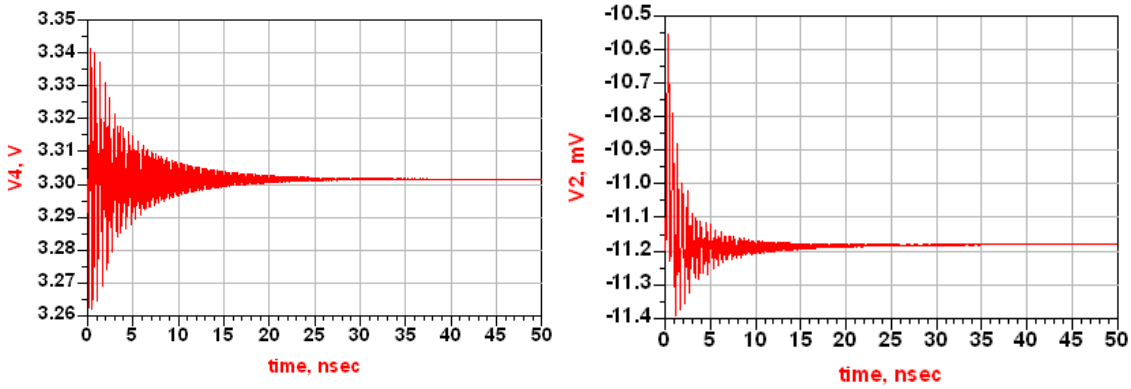


Figure 142 Voltage fluctuations at Port 4 (V4) in left, and at Port 2 (V2) in right for Case 2

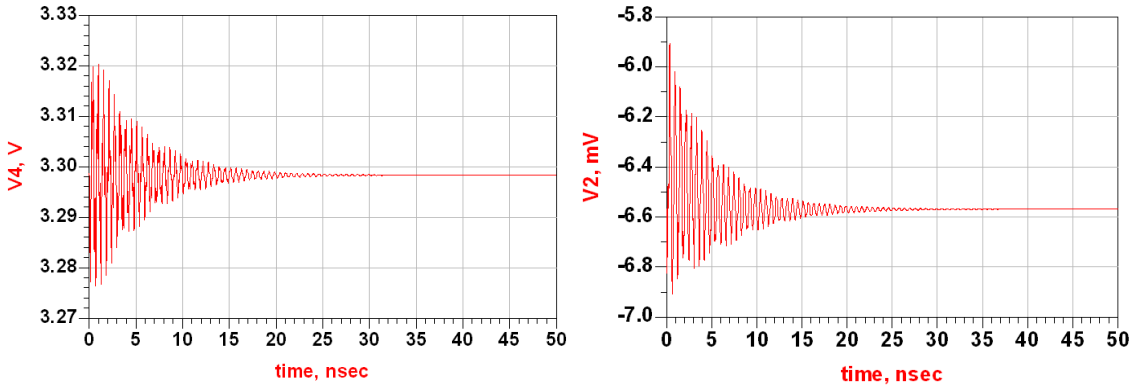


Figure 143 Voltage fluctuations at Port 4 (V4) in left, and at Port 2 (V2) in right for Case 3

5.8. Concluding Remarks

In this chapter, the effect of electromagnetic coupling on the bond-pads of embedded chips when there are excitations in the parallel plate cavity formed by power and ground planes, due to via transitions across the cavity, has been demonstrated through simulations and measurements. When a chip is routed through its package, noise can be induced in the various sections along the route from the bond pads of the chip to the package BGA balls. In the case of embedded actives, noise from the package PDN directly couples to the bond pads in addition to what can get induced along the path through the package. The analysis to estimate accurately any voltage fluctuations at each bond pad of the chip can be very time consuming, considering the fact that, as the functionality supported by the chips increases, the number of I/Os which are in turn the bond pad terminals also increase. The analyses performed and the results from test vehicles indicate the significance of the coupling that is observed and noise voltages

induced at the bond pads of embedded chips corresponding to multiple variations in layer stack-up and proximity of bond pads with excitations on the package PDN.

In this chapter, based on the analysis conducted, the two factors that affect the EM coupling to the bond pads are summarized below.

1. The proximity of the aperture edge on the power planes and the bond pads significantly impact the coupling to the bond pads. This translates to the location of bond pads of the chip. The peripheral bond pads are more prone to the impact of coupling as compared to the interior bond pads. While this is for chips with array area bond pads, in the case of peripheral chips, all the bond pads are equally prone to the impact of EM coupling from the power planes of the package. Also, multiple vias can experience transient currents at various operating conditions of the chip and the coupling experienced by the bond pads needs to be estimated taking these into account.
2. The dielectric thickness of the package is another important factor that determines the magnitude of coupling experienced at the bond pads. Thicker dielectric materials induce voltage fluctuations of larger magnitude at the chip bond pads.

CHAPTER 6

CHIP-PACKAGE INTERACTION IN PACKAGES WITH EMBEDDED CHIPS: ELECTROMAGNETIC COUPLING ON CHIP SUBSTRATE

This chapter deals with the interaction between the EM coupling generated in the package and the bulk substrate of the embedded chip. In Chapter 5, the cavity in the package which houses the embedded chip was left open. However, needs may arise where the cavity needs to be closed with a metal covering and this would expose the chip to even higher levels of noise coupling from the package. Consider the following two scenarios, both of which require the cavity housing the embedded chip to be closed. Proper heat dissipation is an important requirement for the normal functioning of the chip. Mounting conventional heat sinks directly over the thinned and embedded chip can potentially damage the chip. One viable option in the case of packages with embedded ICs is to stamp a metal foil or sheet over the chip that acts as a heat spreader. As it is common practice to ground all exposed metal surfaces to reduce EM radiation [**129**], the metal layer covering the cavity would also be grounded.

Consider another scenario that may require the cavity to be closed. In some chips, especially those that support RF functions, the backside of the chip's bulk substrate is metalized and this serves as the ground. The chip ground and package ground need to be connected with least possible inductance. The current through the ground network of the chip is the summation of source and bulk currents. Inductance of ground network causes

changes in bulk current (dI/dt), which can be significant enough to cause ground noise. Therefore it is important to avoid any variations in the ground potential of the chip and thereby any voltage fluctuations in the chip's ground network due to the inductance associated with the ground path [**69**]. In order to keep the inductance of the ground path as low as possible, the cavity is be covered with a ground plane. This set-up can sometimes result in the chip being enclosed in a cavity between planes of opposite polarity. The goal of this chapter is to analyze such scenarios where the cavity housing the embedded chip is closed with ground metallization.

Now, consider a case as shown in Figure 144 where a chip is embedded within a covered cavity. The figure shows a single bond pad, which is a stand in for the chip fan out. Furthermore, G refers to the ground plane which covers the cavity housing the embedded chip, while P is the power plane in the figure. The plane G also serves to ground the back metallization of the embedded chip. Notice that the on-chip bond pad in the figure is a power pad as it is connected to plane P. Under this condition, the embedded chip shares the ground and the power planes constituting the plane pair cavity.

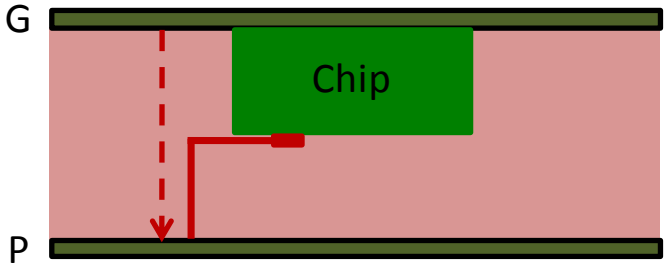


Figure 144 Chip embedded within a covered cavity

Given such a setup, if there are power/ground vias that transition through the plane pair cavity housing the embedded chip, the EM waves radiated from these vias

couple directly with the chip substrate. Now, consider any such excitation across the plane pair cavity GP, which is indicated in the figure using a red arrow with broken line. The presence of this excitation will set up electromagnetic waves in the plane pair cavity GP, which as mentioned before, couple with the embedded chip. Figure 144 is a simple case that illustrates the need to analyze the mechanism of EM wave coupling from the package on to the embedded chip. Such situations require the analysis of how the chip substrate is affected by the EM coupling from the package. This setup is distinguished from other cases analyzed in Chapter 5 in the sense that the bulk substrate of the chip in the earlier cases was not subjected to any interference from the package. But in the setup shown in Figure 144, the chip substrate is enclosed within the plane pair cavity, which means that electromagnetic waves setup in the plane pair cavity GP can now couple with the chip substrate, which was not the case before. Note that the EM waves injected into the bulk substrate affect the proper working of the on-chip active and passive circuits. Therefore, it is important to understand, characterize and quantify the EM coupling impacting the chip substrate in order to take preventive measures. In the following sections, the effect of electromagnetic coupling injected in to the substrate from the package will be analyzed. Before this chip-package interaction is studied in detail, it is important to gain an understanding of wave propagation characteristics of the silicon substrate. In particular, silicon behaves as a semiconductor, dielectric and metal depending on the operating condition of the silicon substrate. Hence, the aforementioned three modes of silicon are first established after which the interaction of embedded chip and package with respect to EM coupling are studied for each of the cases.

6.1. Three Modes of Silicon Substrate

Metal interconnects on silicon substrates exhibit different electromagnetic wave propagation characteristics depending on the resistivity of silicon and the frequency of operation [**130**] [**131**]. In Figure 145, Figure 146 and Figure 147, the various modes of electromagnetic wave propagation exhibited by silicon substrate are shown. Silicon in general can exhibit three modes, namely — slow wave, quasi dielectric and skin effect. In the quasi dielectric mode, silicon behaves like a dielectric. This means that in this mode when there is electromagnetic wave propagation through the substrate, both electric and magnetic fields freely penetrate through the silicon substrate. The permittivity of silicon as a dielectric is between 11.8 and 12. The phenomenon of quasi dielectric mode is generally exhibited in high resistivity silicon. In the slow wave mode, the electric and magnetic fields are decoupled in the sense that the electric fields exists only within the dielectric (oxide) layer above the silicon, while the magnetic field still freely passes through the silicon substrate. In other words, slow wave mode characterizes the semiconductor behavior of silicon. In the skin effect mode, both the electric and magnetic fields do not penetrate through silicon. That is, silicon behaves as a metallic substrate in this mode. Silicon substrates of very low resistivities exhibit this mode where the fields are concentrated only in the dielectric layers above the silicon substrates.

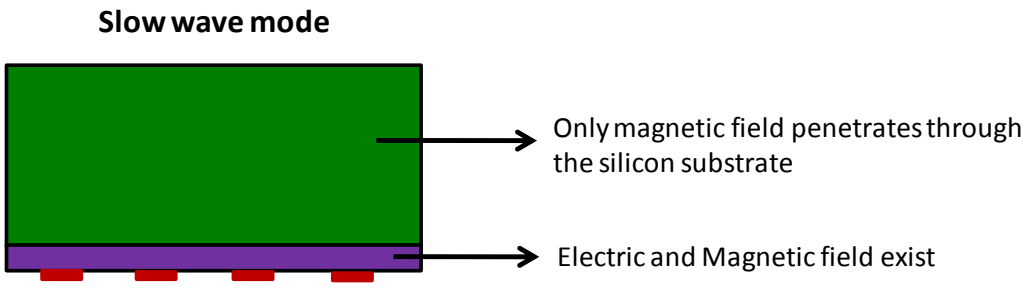


Figure 145 Slow wave mode of propagation in Silicon substrate

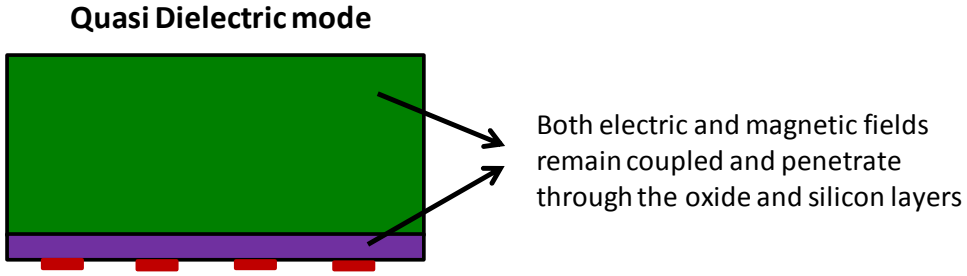


Figure 146 Quasi dielectric mode of propagation in Silicon substrate

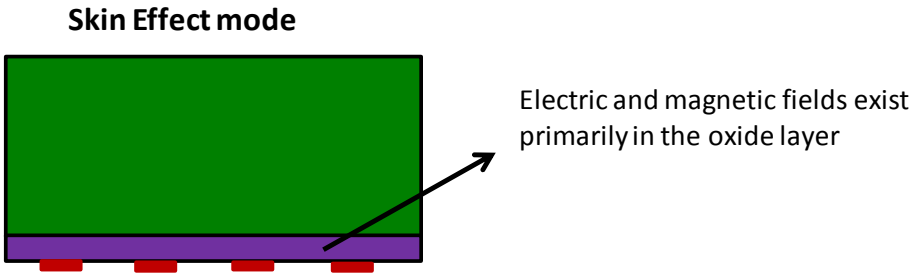


Figure 147 Skin Effect mode of propagation in Silicon substrate

In the above discussion, the different modes are described as being dependant on the conductivity of the silicon substrate used. However, the manifestation of each of these modes in a silicon substrate depends not only on the conductivity of the substrate but also on the frequency of operation, thicknesses of the silicon substrate of the embedded chip and the build-up dielectric layer above the silicon substrate. As the frequency regime under investigation changes, there will be a transformation of the wave propagation behavior of silicon substrate from one mode to another. For example, a silicon substrate

of medium resistivity of 10 Ohm-cm behaves in the slow wave mode in the MHz and lower GHz frequency ranges, but transitions into quasi dielectric mode as the frequency of operation extends further into the GHz frequency range.

In the following, the boundaries of the slow wave mode and quasi dielectric mode are plotted as frequency vs. resistivity charts for varying silicon resistivity and frequency for given thicknesses of silicon substrate and dielectric build-up layer over silicon. The transmission properties of silicon for these various modes have been derived using a parallel plate wave guide model in [**132**]. The frequency region of each mode depends on various parameters, such as substrate conductivity σ_s, thickness t_s, dielectric constant of silicon ε_{si}, thickness of dielectric layer t_d and its dielectric constant ε_d. The dielectric relaxation frequency f_e of silicon, characteristic frequency f_δ for skin effect in silicon layer, relaxation frequency f_s of interfacial polarization and the characteristic frequency f_0 of slow wave mode are given by the following family of equations:

$$f_e = \frac{\sigma_s}{2*\pi*\varepsilon_0*\varepsilon_{si}}$$

$$f_\delta = \frac{1}{\pi*\mu_0*\sigma_s*t_s^2}$$

$$f_s = \frac{1}{2*\pi}*\frac{\sigma_s*t_d}{\varepsilon_0*\varepsilon_d*t_s}$$

$$f_0^{-1} = f_s^{-1} + \frac{2}{3} f_\delta^{-1}$$

In particular, f_e marks the frequency above which the dielectric relaxation takes place where silicon starts to behave as a dielectric material. f_δ is the frequency at which

the skin depth becomes equal to the thickness of silicon substrate. At frequencies above f_δ, the skin depth becomes lesser than the silicon substrate and silicon starts to assume metallic properties. f_0 is the boundary below which the slow wave mode exists. The plot of frequency vs. resistivity shown below is obtained by solving the above equations for various silicon conductivities and silicon/dielectric thicknesses. f_e and f_0 are shown in the frequency vs. resistivity chart.

Now, the wave propagation behavior of silicon is discussed in the context of an embedded silicon chip. When the package needs to support a high fan out density for the embedded chip, it is usually assembled over a thin build-up layer in the order of 20–50 um [**100**]. In Figure 148 below, the cross section of a package, which is 300 um thick consisting of an embedded chip of 280 um thickness is shown. In this case, a 20 um build-up layer supports the chip bond pads. As mentioned earlier, embedding chips on a thin build-up layer, supports high routing and via densities. In Figure 149, the resistivity vs. frequency chart for the cross section shown in Figure 148 is plotted for a build-up layer of 20 um thickness. The frequency limits for the slow wave and quasi electric modes of the silicon substrate are obtained from Figure 149. The region between the slow wave mode and quasi dielectric mode is the transition region where the properties of the silicon substrate gradually transition from one mode to the other. In this region, the silicon substrates behave both in slow wave and quasi dielectric modes in varying degrees that change with frequency.

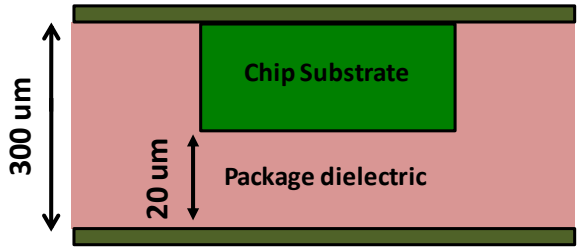


Figure 148 Cross section of embedded chip package with 20 um build-up dielectric below the chip

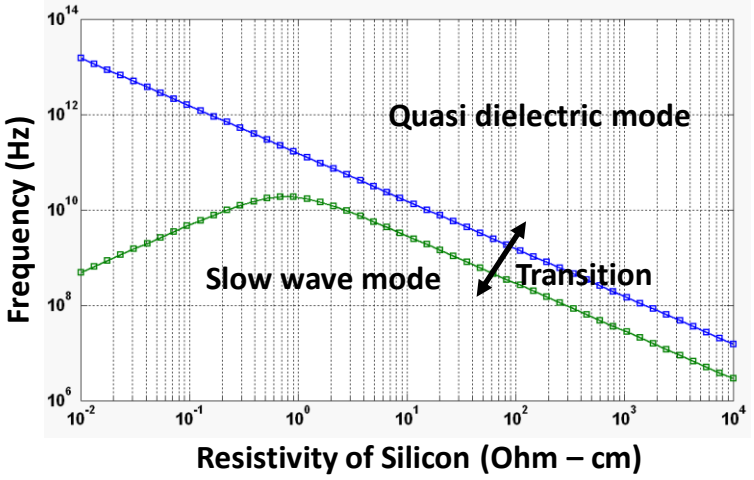


Figure 149 Resistivity vs. Frequency chart for Figure 148

As the thickness of the build-up layer below the chip is increased to 50 um as done in Figure 150, the transition region between the slow wave and quasi dielectric modes of the silicon substrate gets suppressed as shown in Figure 151.

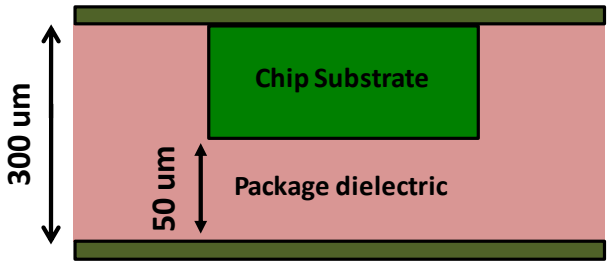


Figure 150 Cross section of embedded chip package with 50 um build-up dielectric below the chip

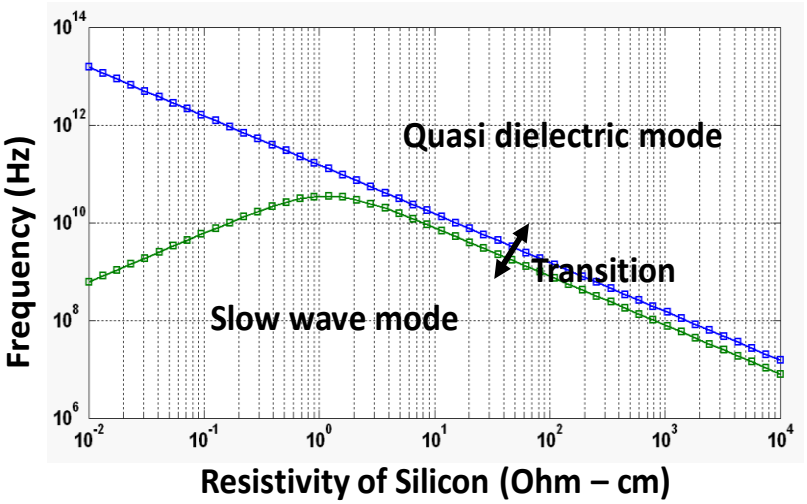


Figure 151 Resistivity vs. Frequency chart for Figure 150

As the thickness of the built up layer is further increased to 100 um (and beyond), as shown in Figure 152, there is an overlap in the boundaries of the quasi dielectric and slow wave modes. This can be as seen in Figure 153, where the transition region is not well defined. As the build-up layer is increased further to 150 um in Figure 154, the transition region extends across the boundaries of the quasi dielectric and skin effect modes as shown in the frequency vs. resistivity chart in Figure 155. This means that the transition region cannot be demarcated as in the case of thin build layers of thicknesses below 50 um.

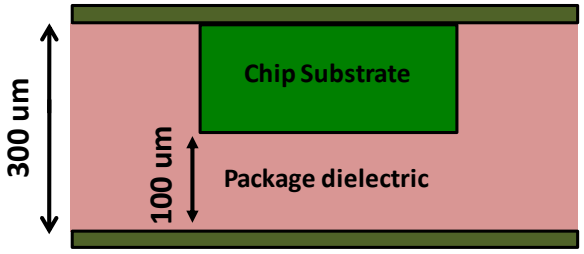


Figure 152 Cross section of embedded chip package with 100 um build-up dielectric below the chip

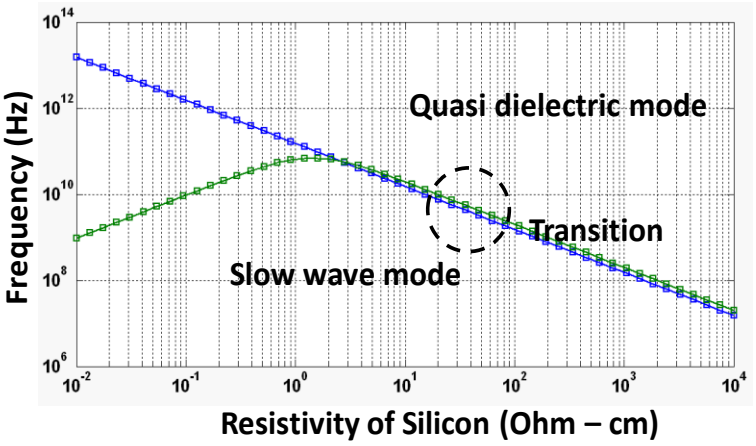


Figure 153 Resistivity vs. Frequency chart for Figure 152

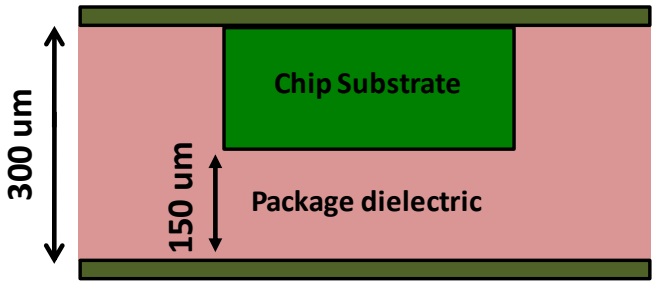


Figure 154 Cross section of embedded chip package with 150 um build-up dielectric below the chip

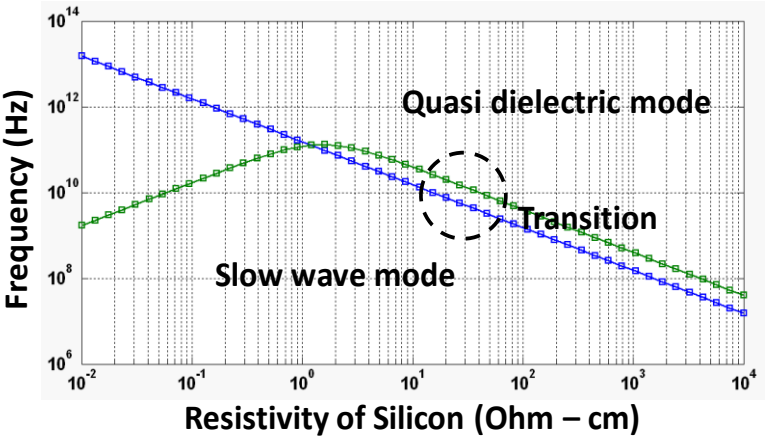


Figure 155 Resistivity vs. Frequency chart for Figure 154

The above frequency vs. resistivity charts for conductivities 1 S/m, 10 S/m, 1000 S/m and 6000 S/m are presented below in a more consumable form that captures the frequency boundaries between the various modes. These conductivities are chosen since the transition from slow wave mode occurs in the frequency range below 10 GHz. Note that the frequency range up to 10 GHz encompasses the operating range of most mobile applications, which is the main focus of this dissertation. Another reason for tabulating the frequency vs. resistivity plots is that later in the section when the behavior of EM wave propagation through the package is analyzed, several frequency points from the transition region would be selected for further study.

6.1.1 Frequency vs. Resistivity Table for 1 S/m

Table 5 tabulates the frequency limits for slow wave and quasi dielectric modes for a silicon substrate of conductivity 1 S/m with varying thicknesses of build-up layer below the silicon substrate. The values in Table 5 are obtained from the resistivity vs. frequency chart plots in Figure 148, Figure 150, Figure 152, and Figure 154 that capture the resistivity/frequency responses for varying build-up dielectric layer thicknesses. Consider a row from Table 5 that deals with a dielectric thickness of 35 um. According to the table, the slow wave mode for this case exists until a frequency of about 480 MHz, while the quasi dielectric mode begins from 1.4 GHz. The intermediate region marks the transition from slow wave to quasi dielectric mode characterized by the penetration of the electric field, which was originally concentrated within the build-up dielectric layer, into the silicon substrate. As per the intrinsic characteristics of slow wave mode, the magnetic field continues to remain unaltered during this transition.

Table 5 Frequency limits for slow wave and quasi dielectric modes for varying dielectric thickness with silicon conductivity of 1S/m

Dielectric thickness (um)	Slow wave mode	Quasi Dielectric
20	0.26 GHz	1.4 GHz
35	0.48 GHz	1.4 GHz
50	0.74 GHz	1.4 GHz
100	1.9 GHz	1.4 GHz
150	3.8 GHz	1.4 GHz

6.1.2 Frequency vs. Resistivity Table for 10 S/m

Similarly, in Table 6 the frequency limits for slow wave and quasi dielectric modes have been tabulated for a silicon substrate of conductivity 10 S/m. This example shows the frequency boundaries between the two modes as the thickness of the dielectric material increases from 20 um to 150 um. Notice that in Table 6, the rows corresponding to dielectric thicknesses in the 20–50 um range have been highlighted as they have a well defined transition region. But for dielectric thicknesses greater than 50 um, the slow wave and the quasi dielectric modes overlap resulting in no clear transition region between them.

Table 6 Frequency limits for slow wave and quasi dielectric modes for varying dielectric thickness with silicon conductivity of 10 S/m

Dielectric thickness (um)	Slow wave mode	Quasi Dielectric
20	2.8 GHz	15 GHz
35	4.7 GHz	15 GHz
50	7 GHz	15 GHz
100	19 GHz	15 GHz
150	38 GHz	15 GHz

6.1.3 Frequency vs. Resistivity Table for 1000 S/m

In Table 7 the limits of the slow wave mode for a silicon conductivity of 1000 S/m are shown. The total thickness of the package is 300 um and the silicon thickness is varied from 150 um to 280 um. As the frequency extends beyond the limits of the slow wave mode, the silicon material starts to assume metallic properties thereby going into skin effect mode.

Table 7 Frequency limit for slow wave mode for varying dielectric thickness with silicon conductivity of 1000 S/m

Dielectric thickness (um)	Slow wave mode
20	4.77 GHz
35	5.36 GHz
50	6.03 GHz
100	9.45 GHz
150	16.82 GHz

6.1.4 Frequency vs. Resistivity Table for 6000 S/m

In Table 8 the limits of the slow wave mode for a silicon conductivity of 6000 S/m are shown. Similar to Table 7, the package thickness is kept at 300 um and the silicon thickness is varied from 150 um to 280 um. As the conductivity increases, the transition from slow wave to skin effect mode begins at a much lower frequency compared to the previous case of 1000 S/m. This can be observed by comparing corresponding rows from Table 7 and Table 8.

Table 8 Frequency limit for slow wave mode for varying dielectric thickness with silicon conductivity of 6000 S/m

Dielectric thickness (um)	Slow wave mode
20	0.81 GHz
35	0.9 GHz
50	1.01 GHz
100	1.58 GHz
150	2.81 GHz

6.2. Embedded Chip Model for Study of Chip Substrate-Package interaction

To develop an understanding of the chip-package interaction phenomenon, a simplified model for the embedded chip is needed. This is because in real test vehicles it may not be possible to capture as many parametric variations as simulations. So, there is a need to come up with a simple yet realistic model of an embedded chip in order to study the interaction between the bulk substrate of the embedded chip and the package. In Figure 156, a flow leading from a commercial chip to an embedded chip model is shown.

The different steps in Figure 156 are labeled A–D. In step A of Figure 156, the chip model consists of the silicon substrate and alternating metal and oxide layers formed over the silicon substrate. This model represents a commercial chip with four to eight metallization layers. The drawback of using this model for the analysis is that it involves an embedded chip that has a high level of complexity. A more simplified model would be required where the focus of analysis is primarily on the interaction with the substrate of the embedded chip. Based on this, as in Figure 156, the chip model is progressively simplified through steps B–D. Moreover, as the chip model gets more and more complicated, it would get harder to understand the interaction between the chip and package and the associated phenomena. In others words, if the chip model consists of several components, one is not sure if the phenomena being observed is the result of the interaction between the package and chip substrate, or due to the additional components involved in the chip model.

Step B of the simplification performed on the chip model in step A is that the various metallization and oxide layers are collapsed into one metallization layer. The rationale behind this simplification is that the focus of the analysis does not involve on-chip circuitry so a primitive representation of the on-chip metallization using a single layer is sufficient for the purposes here.

In step C of Figure 156, the simplified one metal layer chip model has been embedded within a cavity in the package dielectric. This cavity is filled with an under fill material which is depicted in yellow color. Moreover, the chip substrate is grounded through the back metallization.

Now, this embedded chip model is further simplified in step D of Figure 156. The simplification from step C to D is based on the following rationale. For modeling purposes, the under-fill can be the same dielectric material that forms the package build-up layers. Also, the on-chip oxide and metallization layers are not considered since most of the EM wave penetration from the package occurs from the sides of the chip substrate. The bulk substrate accounts largely for the chip thickness as compared to the oxide and metallization layers and hence has a significant influence on the coupling across the package plane pair cavity. Therefore, step D is suitable enough to investigate the phenomenon under consideration.

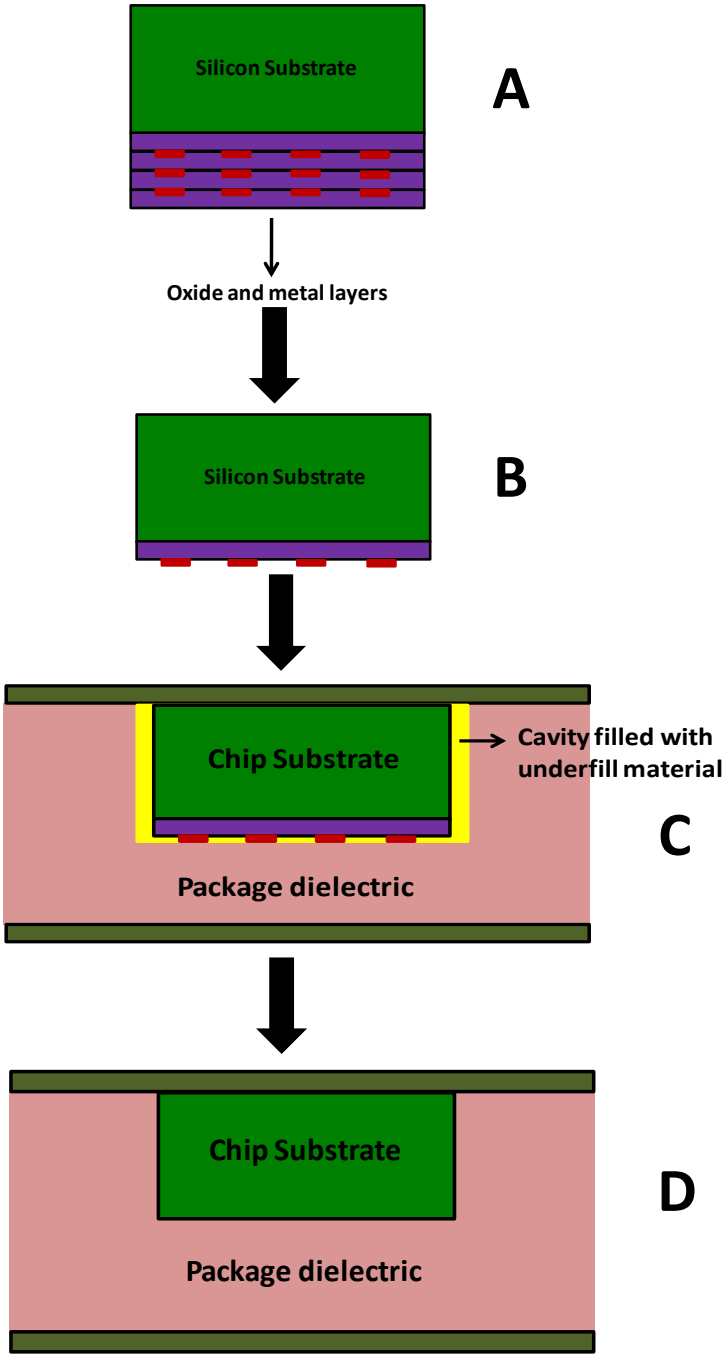


Figure 156 Embedded chip used for substrate coupling analysis

Figure 157 shows the model from step D of Figure 156. This model is used for EM simulations to analyze the effect of coupling of electromagnetic waves from the package to the silicon substrate of the embedded chip. The model consists of a plane pair

cavity formed by a power P and ground G plane, with the chip embedded in the center of the package. The package dielectric material used for simulation here is FR–4 with a dielectric constant of 4.5 and loss tangent of 0.01. Ports 1 and 2 mark the excitation and the response points of the package, respectively. The coupling between the two ports is measured for various chip size/thicknesses. Moreover, the impact of silicon conductivity on the EM wave propagation through the packages is analyzed using simulation results. The dielectric permittivity of embedded silicon used in the simulation is 11.8.

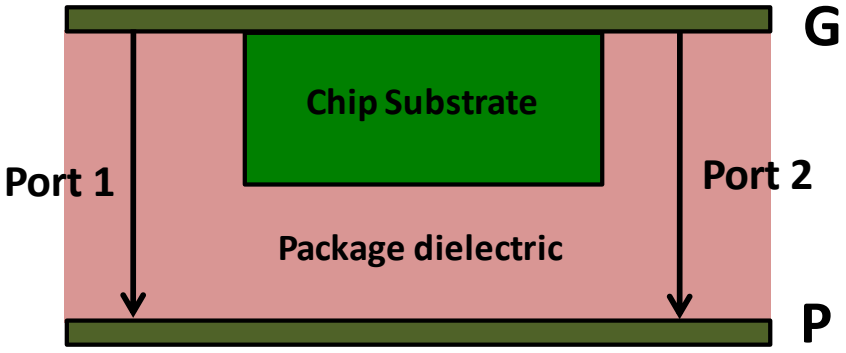


Figure 157 Model used for EM simulation

Silicon substrates of various resistivities are included in the EM simulation analysis to understand the effect of EM coupling on high, medium, and low regimes of silicon resistivity. In general, silicon of different resistivities is used in different application scenarios. For example, CMOS process uses low resistivity silicon (i.e., high conductivity) spanning the range of 1–3 Ohm-cm [**131**]. In recent times, high resistivity grade silicon is gaining popularity since it is seen as an effective measure to suppress on-chip substrate coupling [**133**]. Also, very low resistivity silicon substrate of about 1 mOhm-cm with an epitaxial layer of resistivity of 10–15 Ohm-cm is also used to fabricate mixed signal chips [**134**]. For the analysis here, in the high resistivity regime, a

conductivity value of 1 S/m is used as a representative. In the mid resistivity regime, a conductivity value of 10 S/m is chosen and in the low to very low resistivity regime, conductivity values of 1000 S/m and 6000 S/m are used. Considering a wide gamut of applications that use silicon substrates spanning a large resistivity spectrum, it is necessary to analyze the effect of EM coupling on silicon substrate of low, medium and high resistivity ranges.

6.3. Substrate Coupling in Silicon of Low Conductivity: 1 S/m

In this section, a silicon substrate with conductivity 1S/m is used for the analyses. The effect of embedded silicon is felt in the coupling across the package when the ratio of the width/length of the package to the width/length of the embedded silicon is lesser than 2.5. For example, Figure 158 shows an embedded chip of width 2a in a package of width W. Note that if W/2a >2.5, the effect of embedded silicon on the transverse coupling across the package is not well pronounced, although EM waves generated in the package still couple to the silicon substrate. In the analysis performed here, different sizes of packages with varying silicon chip dimensions are used. In Figure 159, the simulation results from a package of lateral dimension of 15 X 15 mm (i.e., W = 15) and thickness 300 um consisting of an embedded silicon of size 4 X 4 mm (i.e., a = 2) and varying thicknesses ranging from 150 um and 280 um, are shown. The transition region from slow wave to quasi dielectric mode in Figure 159 spans across the MHz region, while the quasi dielectric mode begins at 1.4 GHz. From the responses it can be seen that the silicon substrate behaves as a dielectric material where the various curves in the plot follow each other closely. The reasons for this behavior can be attributed to the quasi

dielectric mode of operation of the silicon substrate as well as the W/2a ratio being 3.75. Hence, the embedded silicon does not have a significant influence on the frequencies and magnitudes of the resonances of the package.

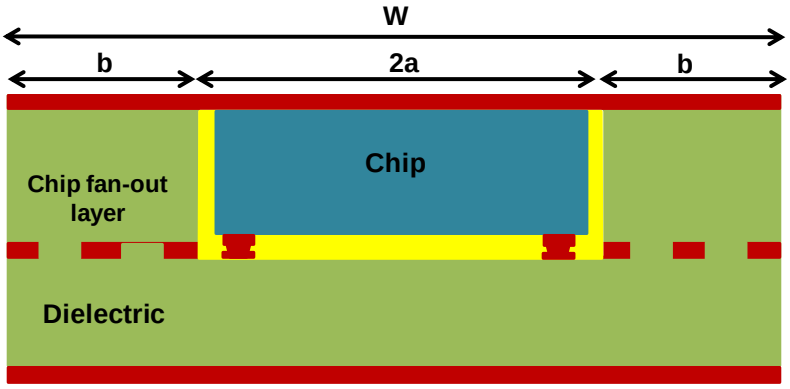


Figure 158 Embedded chip of width '2a' in a package of width 'W'

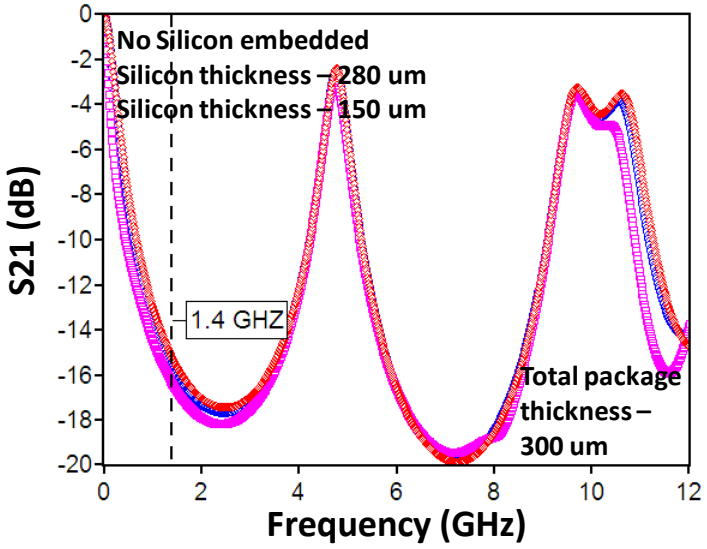


Figure 159 Isolation across Ports 1 and 2 (S21 in dB) for a 15 X 15 mm package with 4 X 4 mm embedded silicon

Next, consider Figure 160 where a larger silicon substrate (7 X 7 mm) is embedded, i.e., 2a = 7. In this case, the responses shown in the graph are from two different thicknesses of embedded silicon, i.e., 280 um and 250 um. Recall from before

that the 4 X 4 mm silicon substrate did not have much influence on the package resonances when it was embedded within a 15 X 15 mm package. Note that in the figure below the blue curve denotes a package that is homogeneously filled with FR–4.The resonances in the responses with silicon chip embedded do not align exactly with that of the case where no chip is embedded. The reason for this effect can be explained as follows. Silicon behaves as a dielectric material in the quasi dielectric mode. Since the permittivity of silicon at 11.8 is higher than that of FR–4 at 4.4, the effective permittivity of the entire package (including the embedded silicon) is higher than that of a package consisting only of FR–4. Moreover, the frequencies at which the resonances occur depend on the effective permittivity of the package. Notice that the resonant frequencies for the package with no embedded silicon exhibits resonance in the ranges of 9–10 GHz, and 10–11 GHz, but in the case with an embedded silicon substrate the resonance occurs only between 9–10 GHz. This is because the effective permittivity of the package influences the frequency of occurrence for each parallel plate cavity mode. Finally, the W/2a value is another reasonable estimate that determines if the embedded silicon would influence the package resonances in the low and mid conductivity regimes. Although, the value of W/2a that starts to affect the package resonances, depends on the conductivity of the embedded silicon. For example, as the conductivity increases to over 100 S/m, smaller silicon sizes with ratios greater than 2.5 starts to influence the package responses.

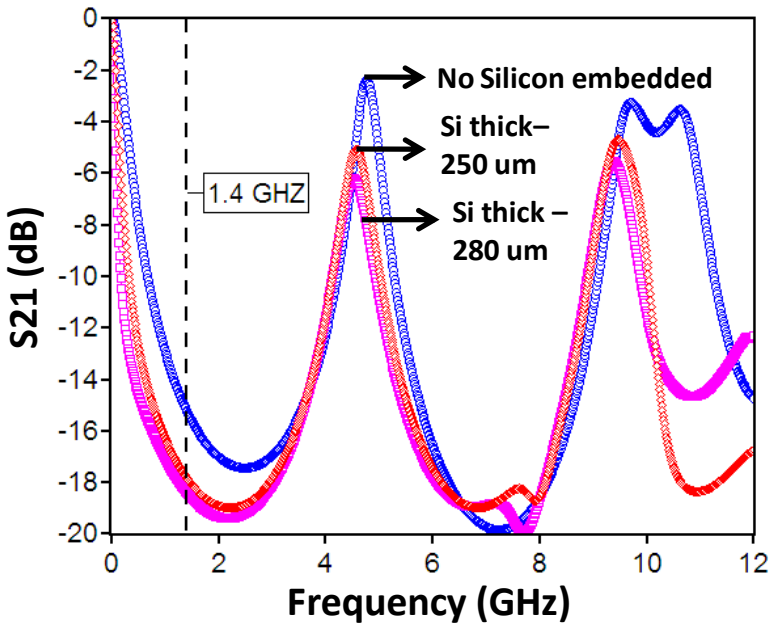


Figure 160 Isolation across Ports 1 and 2 (S21 in dB) for a 15 X 15 mm package with 7 X 7 mm embedded silicon

Next the size of the silicon chip is further increased to 10 X 10 mm in Figure 161. Simulation results for substrates of thicknesses 150 um, 250 um and 280 um are shown. As the proportion of embedded silicon within the package increases, the influence of silicon substrate on EM wave propagation through the package increases. For a silicon substrate of thickness 280 um embedded within a package of 300 um, there is a considerable shift in the resonant frequency points and the losses associated with the silicon substrate suppresses the magnitude of the resonant peak as compared to the case of a package with no embedded silicon. This effect can be observed by comparing the red and green curves in Figure 161.

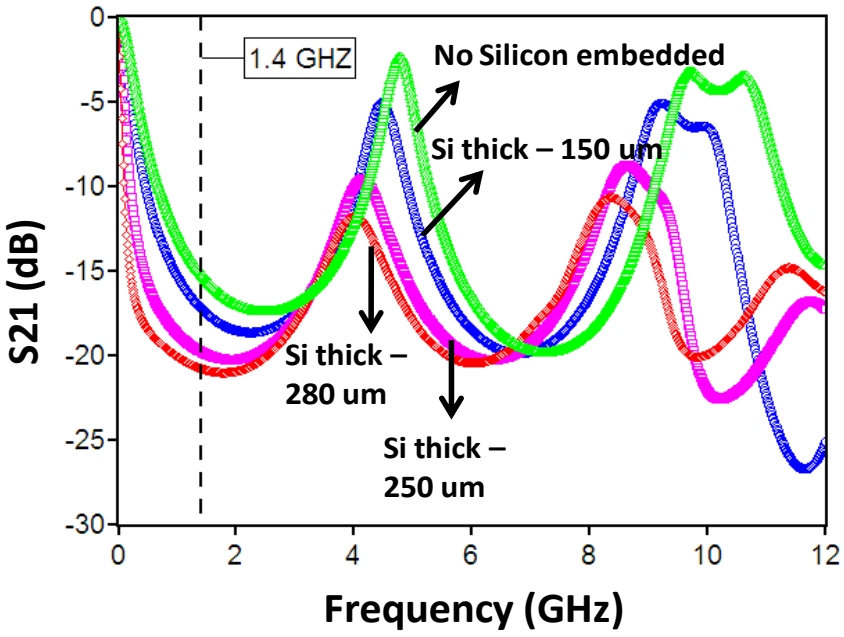


Figure 161 Isolation across Ports 1 and 2 (S21 in dB) for a 15 X 15 mm package with 10 X 10 mm embedded silicon

In the three cases discussed above, the effect of the size and thickness of the embedded silicon substrate on the package resonances has been analyzed. As the thickness and size of the embedded silicon increases, the frequencies of resonance gets shifted to lower values and the loss due to the embedded silicon reduces the magnitude of the resonances observed.

Now, to better understand the mode of propagation exhibited by the embedded silicon, the electric and magnetic fields across various locations of the package cross sections are plotted. This field distribution gives an idea of the extent of penetration of fields into silicon substrate, using which the modes of silicon can be deduced. In all field plots in this chapter, the cross-sections are sampled at different values of X, which is the axis along which the width of the package is aligned.

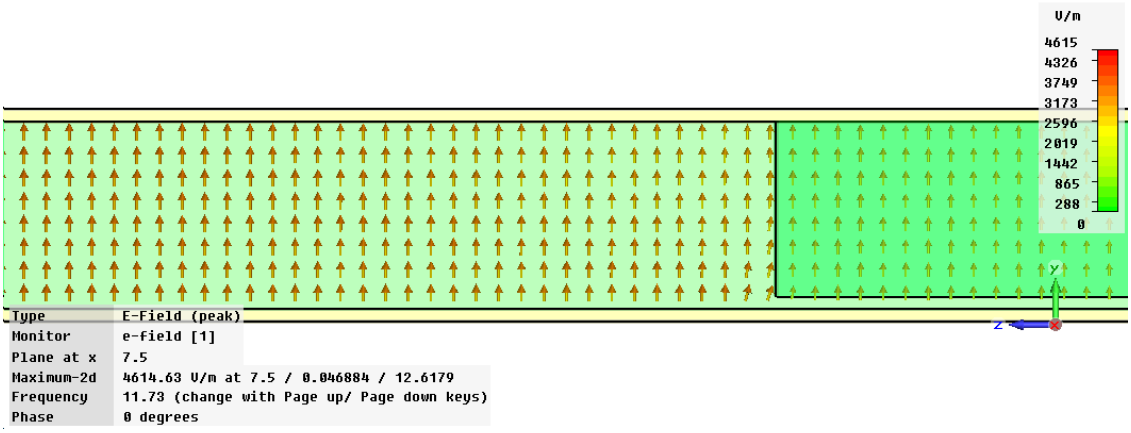


Figure 162 E-Field at cross section X = 7.5 mm and frequency 11.73 GHz

Figure 162 shows a vector plot of the electric field at cross section X = 7.5 mm and a frequency of 11.73 GHz. In Figure 163, a closer view of the E-field vector plot is shown along with the top ground plane. The cross section is made at the region where silicon is embedded. In the figure, the silicon and the dielectric regions along with their interface are labeled. The vectors of the E-field are vertically directed between the top and bottom planes as is expected in packages where the thickness of the dielectric build-up layers is much smaller as compared to the lateral dimensions. An important point to note here is that the vector field distribution is uniform across the dielectric, silicon and their interfaces. Since the E-field freely penetrates through the silicon substrate (in the same way it does to a dielectric material), the propagation mode supported by the silicon substrate is concluded as being quasi dielectric mode. As per the calculation in the frequency/resistivity chart in Table 5, the quasi dielectric mode is supposed to begin at a frequency of 1.4 GHz. Hence at a high frequency value (i.e., 11.73 GHz), the E-field plot in Figure 163 shows a condition where the silicon is in true quasi dielectric mode.

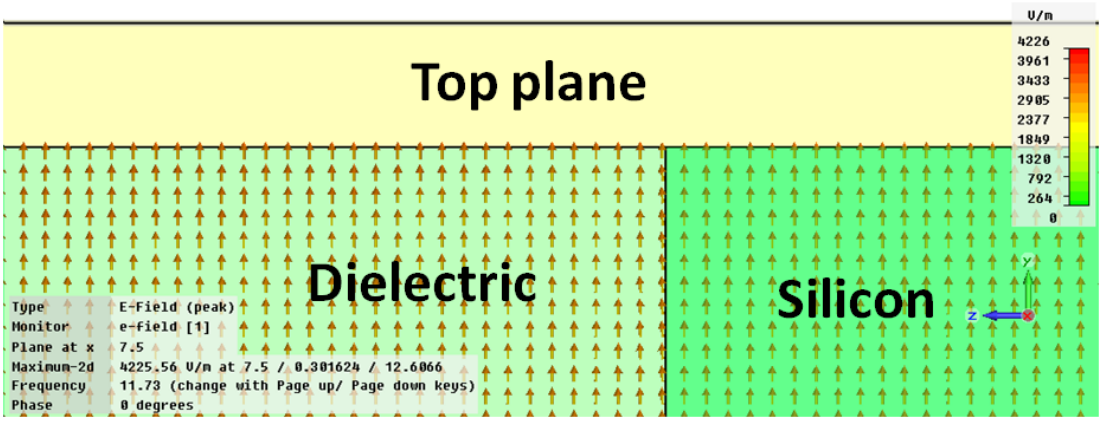


Figure 163 Closer view of Figure 162 showing E-field distribution at the chip and package interface near the top plane (G Plane)

In Figure 164, the E-field distribution in the vicinity of silicon dielectric interface near the bottom plane is shown. Note that this is the same cross section as in Figure 163. In this case it can be seen that the E-field is more concentrated in the dielectric region than in the silicon region. Still there is significant penetration of E-field through the silicon substrate although not at the same concentration levels as in the dielectric regions.

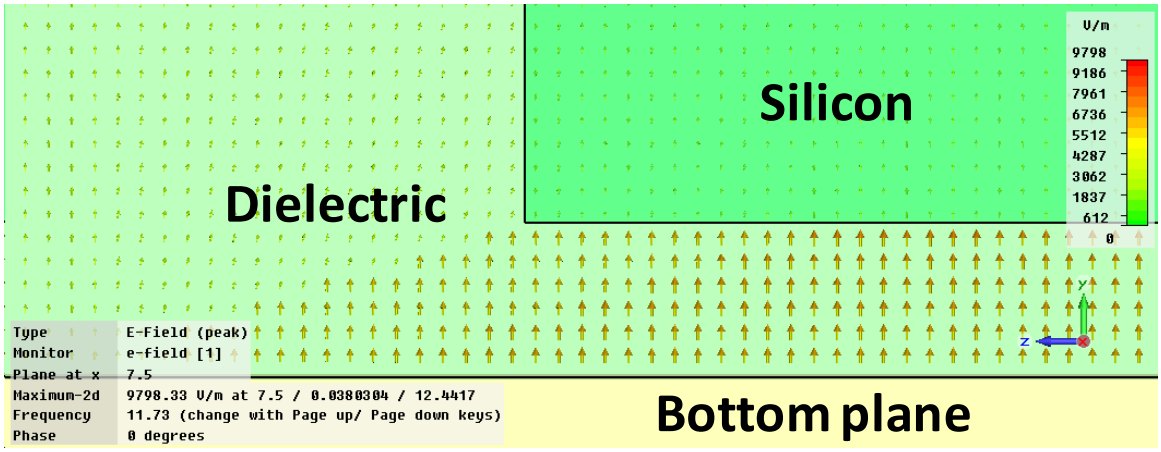


Figure 164 Closer view of Figure 162 showing E-field distribution at the chip and package interface near the bottom plane (P Plane)

In the following three figures, the magnetic field distribution across the package at various cross section and frequencies are shown. In Figure 165 the vector plot for the magnetic field distribution at cross section X = 2 mm is shown and at a frequency of 10.175 GHz. Note that X = 2 mm captures the magnetic fields outside of the region where die is embedded. Therefore, it is not surprising that the magnetic field distribution as seen from the figure is uniform across the cross section of the package due to the homogeneity of the dielectric in the cross section.

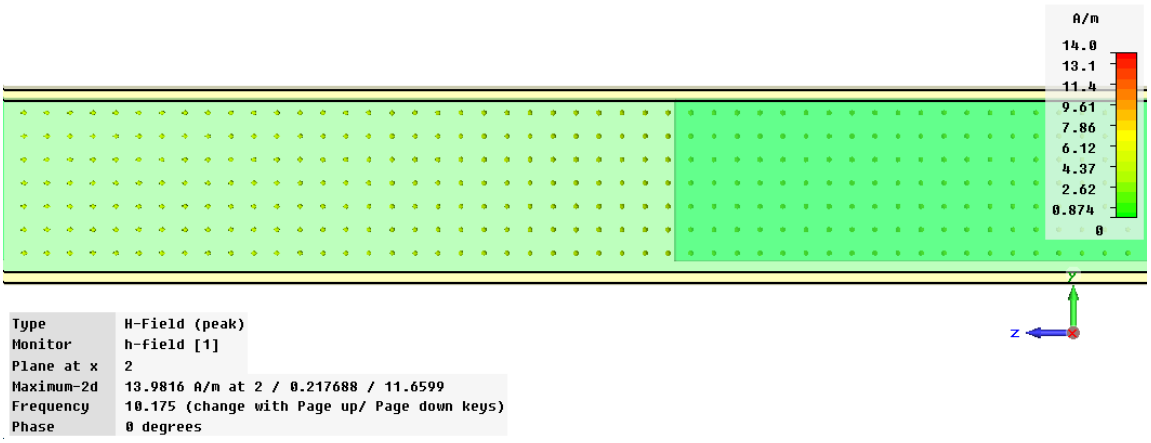


Figure 165 H-Field at cross section X = 2 mm and frequency 10.175 GHz

Now, the magnetic field distribution is analyzed in the region where the die is embedded. In Figure 166 and Figure 167, the cross section is made at X = 7.5 mm and at a frequency of 11.73 GHz. Figure 167 is a zoomed in view of the magnetic field distribution at the interface of the silicon and dielectric in the vicinity of the bottom plane. As seen from the figures, the magnetic field freely penetrates through the silicon, which indicates that the propagation mode supported by the silicon substrate is quasi dielectric.

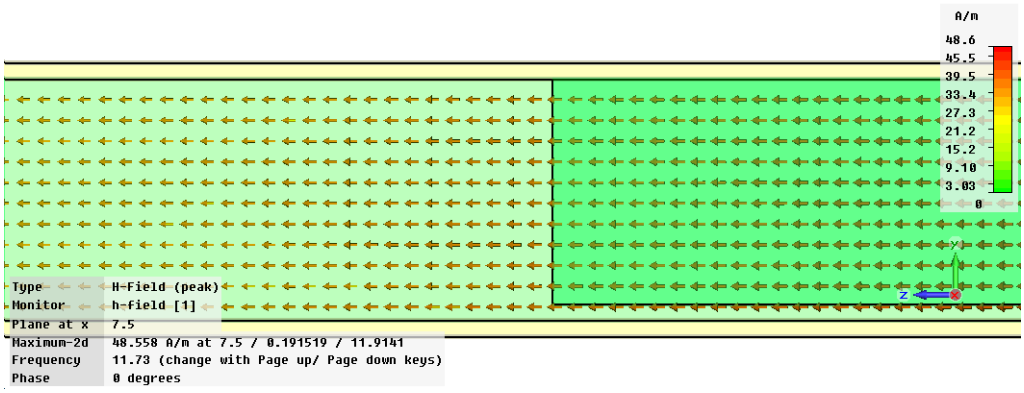


Figure 166 H-Field at cross section X = 7.5 mm and frequency 11.73 GHz

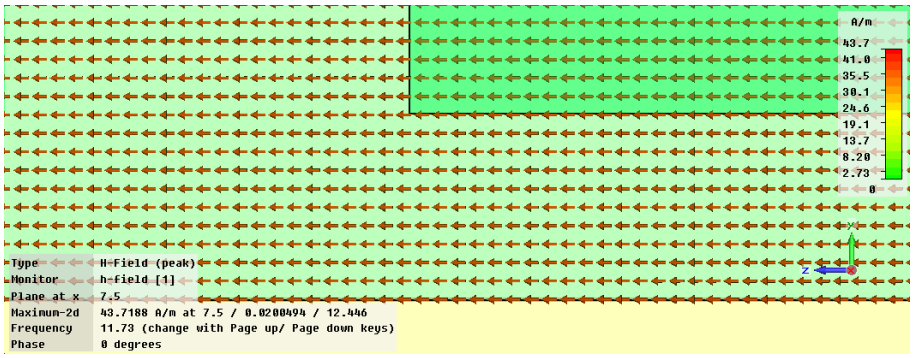


Figure 167 Closer view of Figure 166 showing H-field distribution at the chip and package interface near the bottom plane (P Plane)

It can be concluded from the E-field and the H-field made at the cross section at X = 7.5 mm and frequency 11.73 GHz in Figure 162 and Figure 166 that the silicon substrate at this frequency is in quasi dielectric mode.

6.4. Substrate Coupling in Silicon of Medium Conductivities: 10 S/m

In this section, silicon substrates with conductivities of 10 S/m is chosen as representative of the mid resistivity regime. Two cases are analyzed, one with embedded

silicon of size 4 X 4 mm and another of size 7 X 7 mm. As in the case with high resistivity silicon, the die size of 4 X 4 mm in a package size of 15 X 15 mm does not influence the frequencies and magnitudes of the package resonances considerably. In Figure 168, the isolation across Ports 1 and 2 for the silicon of thicknesses 250 um and 280 um is shown for embedded silicon of size 4 X 4 mm, while in Figure 169 the same response is shown for silicon of thicknesses ranging from 150 um to 280 um for silicon of size 7 X 7 mm. For a given package thickness, as the thickness of the embedded silicon increases, the resonance peaks in the isolation response are suppressed due to the losses in silicon substrate. If there is a thick build-up layer below the silicon of thickness greater than 50 um, the electric and magnetic fields in the build-up region support the propagation of electromagnetic waves due to which the resonances become more and more pronounced. In Figure 168 and Figure 169, the boundary for the slow wave mode for various thicknesses of embedded silicon is marked by dotted lines. This phenomenon is further explored by plotting the E and H-field vectors for silicon of thickness 280 um by choosing frequencies that fall within the slow wave region, and from the transition region in Figure 168 and Figure 169.

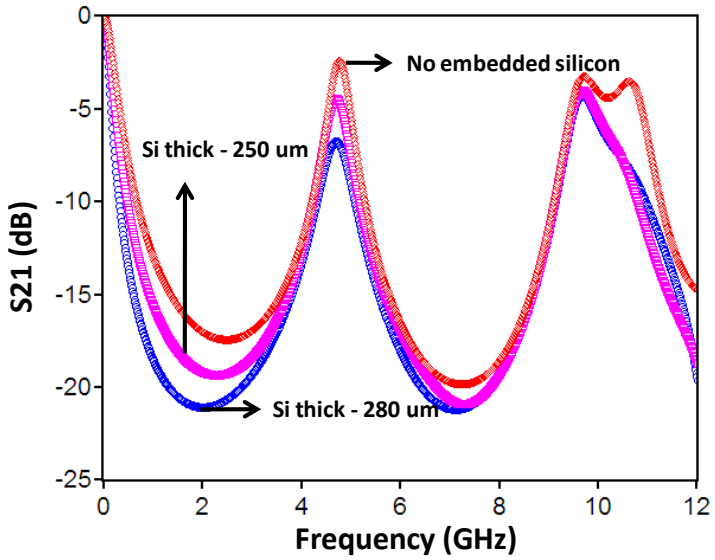


Figure 168 Isolation across Ports 1 and 2 (S21 in dB) for a 15 X 15 mm package with 4 X 4 mm embedded silicon

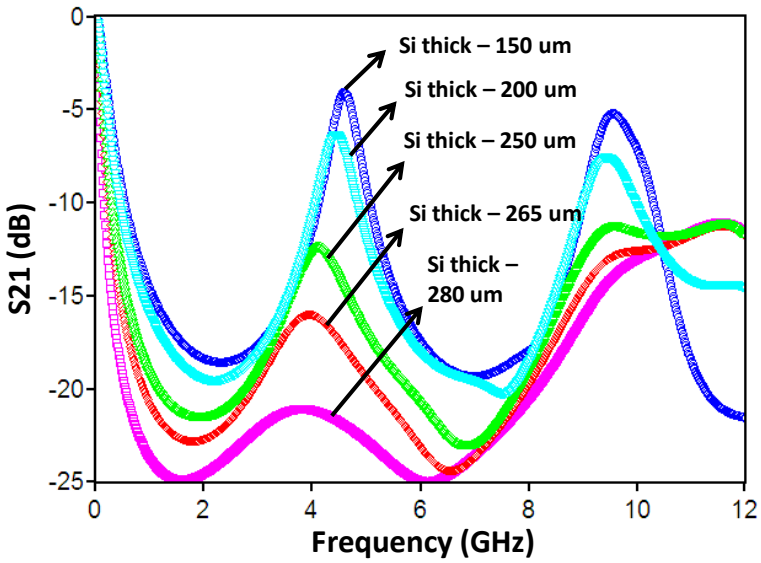


Figure 169 Isolation across Ports 1 and 2 (S21 in dB) for a 15 X 15 mm package with 7 X 7 mm embedded silicon

First of all, the E-field vector is plotted at the cross section of X = 2 mm and a frequency of 4.5 GHz, which is shown in Figure 170. As the cross section is made

outside the region of embedded silicon, the E-field distribution is uniform throughout. But in the case of cross sections made at X = 7.5 mm as shown in Figure 171 and Figure 172, the E-field distribution is concentrated in the dielectric region below the embedded silicon. At the interface between the silicon and dielectric (i.e., on the sides of the embedded silicon), the E-field vectors align themselves normally to the interface. Here the penetration of E-field through the silicon is therefore suppressed.

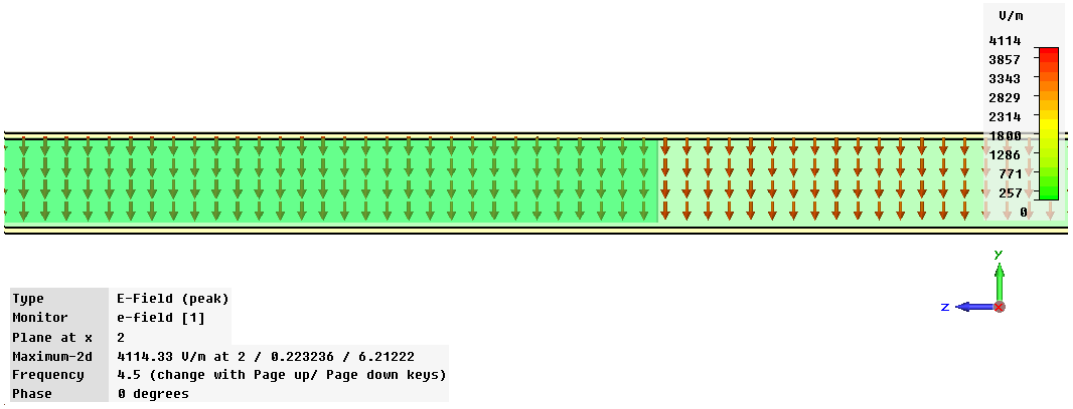


Figure 170 E-field plot at cross section X = 2.0 mm and frequency 4.5 GHz

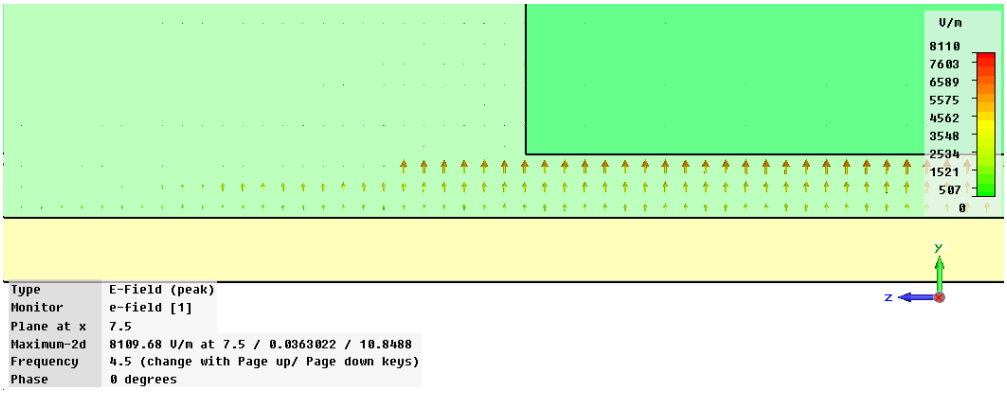


Figure 171 E-field plot at cross section X = 7.5 mm and frequency 4.5 GHz

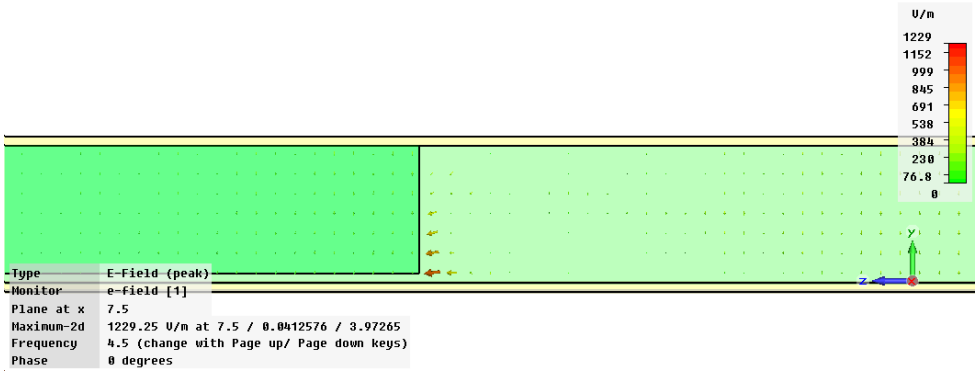


Figure 172 Closer view of the silicon and dielectric interface showing E-field plot at cross section X = 7.5 mm and frequency 4.5 GHz

Next, the magnetic field distribution at the same cross sections of X = 2 mm and X = 7.5 mm are considered for analysis. Figure 173, Figure 174 and Figure 175 show uniform magnetic field distribution in the region where the dielectric is homogeneous (no embedded silicon), and also where the silicon is embedded. A closer view of the cross section with embedded silicon is shown in Figure 175, where it can be seen that the H-field vectors are uniformly distributed indicating the existence of slow wave mode of the embedded silicon.

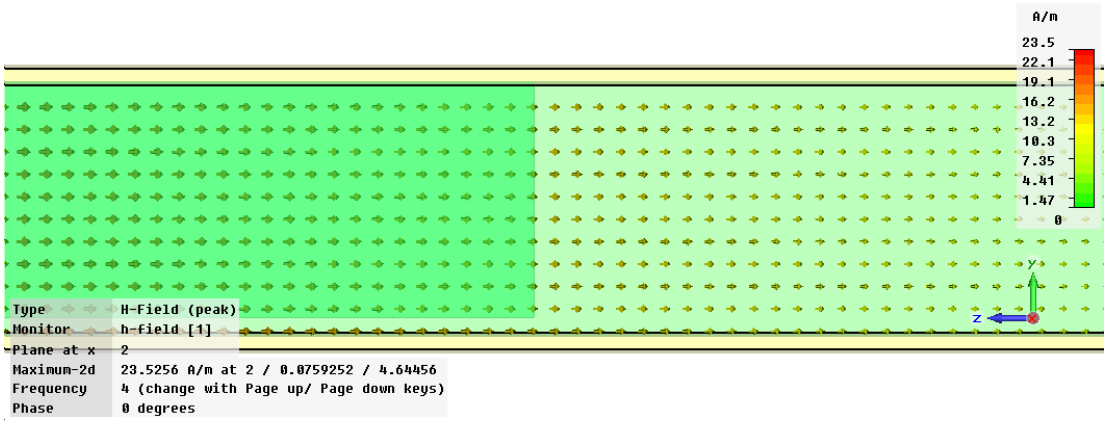


Figure 173 H-field plot at cross section X = 2.0 mm and frequency 4 GHz

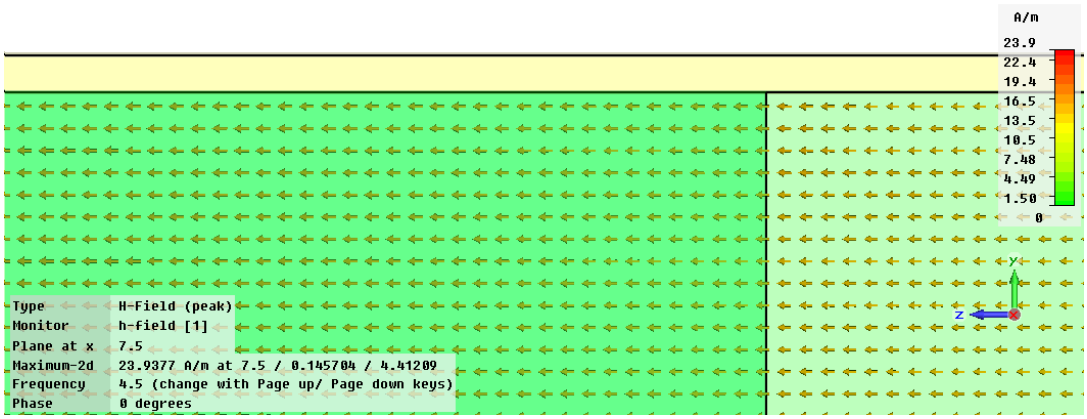


Figure 174 H-field plot at cross section X = 7.5 mm and frequency 4.5 GHz

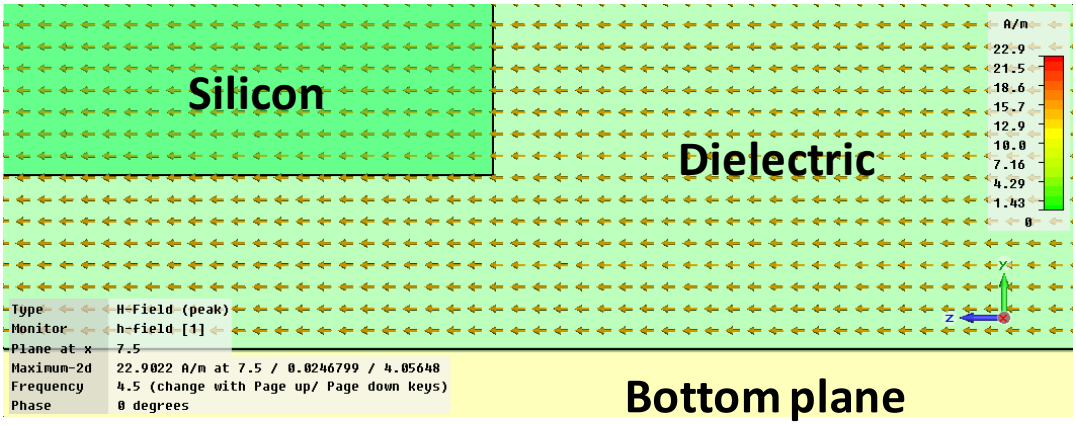


Figure 175 Closer view of the H-field distribution plot at cross section X = 7.5 mm and frequency 4.5 GHz

To summarize, the package resonances are suppressed due to the losses in the silicon substrate and the mode of wave propagation exhibited by the silicon substrate is determined from the frequency of operation, silicon conductivity and thickness of the dielectric layer. For medium conductivities such as 10 S/m, at higher frequencies the transition from slow wave to quasi dielectric mode is characterized by the penetration of

E-field. The increase in material loss for silicon substrates as the conductivities increase, results in the suppression of resonances.

6.5. Substrate Coupling in Silicon of High Conductivity: 1000 S/m

For silicon substrates of high conductivities, the behavior of the embedded silicon when transitioning from slow wave to skin effect mode is examined in detail. First, silicon substrate of conductivity 1000 S/m is considered in the frequency range extending from dc to 12 GHz. This frequency range is chosen so as to capture the transition from slow wave to skin effect mode. Recall that in the slow wave mode only the magnetic field penetrates through the silicon substrate, while in the skin effect mode neither the magnetic nor the electric fields penetrate the silicon as it behaves like a metal. The electric and magnetic fields are captured at various frequency points within two frequency bands, one extending up to 5 GHz and the other spanning 7–12 GHz. These two frequency bands describe the behavior of the silicon substrate in slow wave mode and its subsequent transition into the skin effect mode. In the slow wave mode the resonances in the S-parameter transfer responses are suppressed and they start to reappear as the silicon moves into the skin effect mode. The package size used for analysis in all the following sections is 15 X 15 mm with an embedded chip of size 7 X 7 mm. The total thickness of the package is 300 um and that of the embedded chip is 280 um.

6.5.1 1000 S/m Slow wave mode up to 5 GHz

In Figure 176, the electric field distribution is plotted at cross section X = 7.5 mm and at a frequency of 100 MHz. From earlier observations the silicon substrate is expected to exhibit slow wave mode in the MHz frequency ranges. So as seen in the E-

field distribution plot, there is no significant E-field penetration within the silicon substrate. The E-field vectors in the vicinity of the silicon/dielectric interface incline towards (or point away) from the silicon edge. Figure 177 shows a closer view of the E-field distribution in the vicinity of the bottom plane. It can be seen that E-field gets heavily concentrated in the dielectric region below the silicon substrate with very little field penetrating through the silicon.

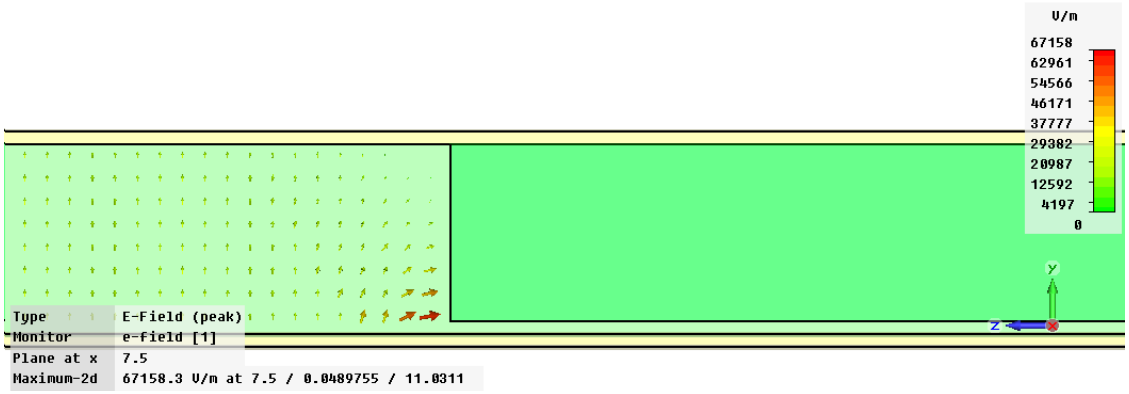


Figure 176 E-field plot at cross section X = 7.5 mm and frequency 100 MHz

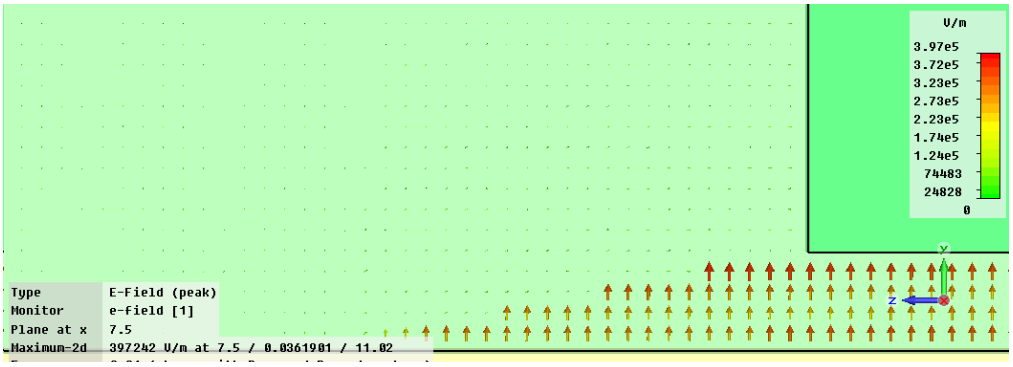


Figure 177 Closer view of Figure 176 showing E-field distribution at the chip and package interface at cross section X = 7.5 mm and frequency 100 MHz

Figure 178 shows the electric field distribution at cross section X = 3.0 mm and at a frequency of 100 MHz. Since this cross section is at a region that is outside the embedded silicon, the E-field distribution is uniform throughout.

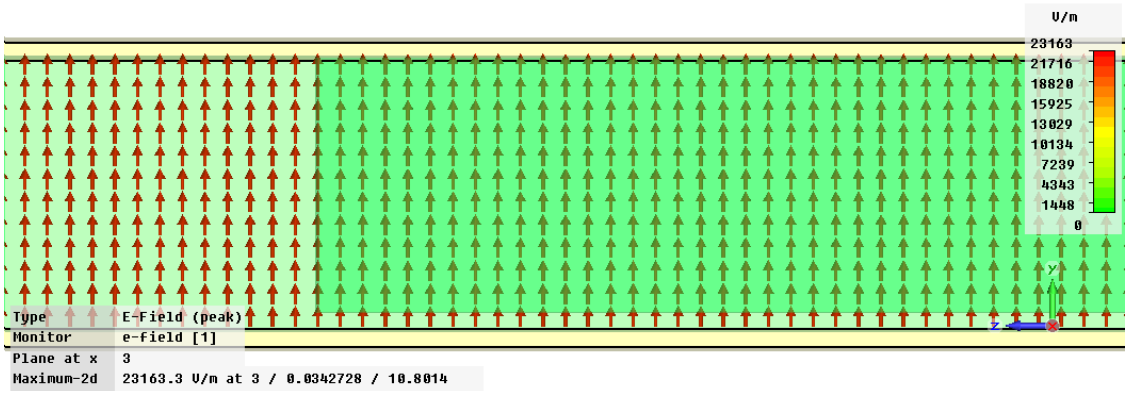


Figure 178 E-field plot at cross section X = 3.0 mm and frequency 100 MHz

In Figure 179, the electric field distribution is plotted at cross section X = 3.0 mm and at a frequency of 5 GHz. This plot shows that the E-field remains uniformly distributed in the region outside the embedded silicon for all frequencies.

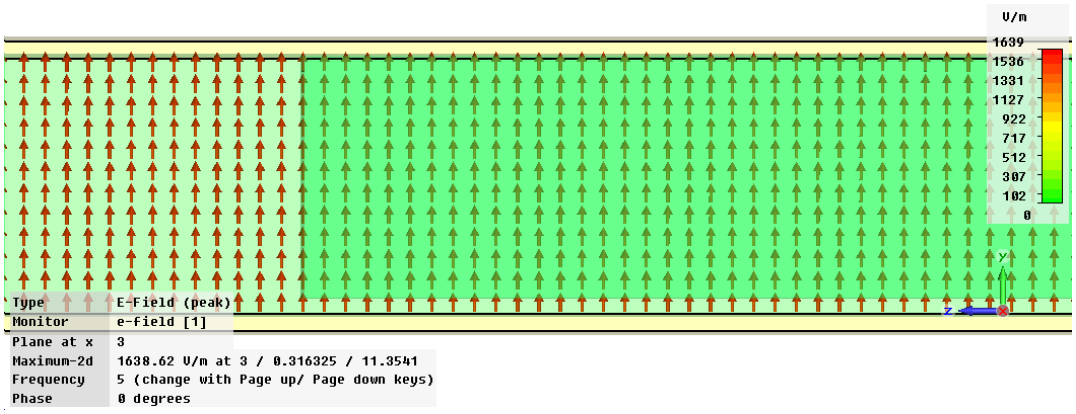


Figure 179 E-field plot at cross section X = 3.0 mm and frequency 5 GHz

In the remainder of this subsection, H-field distribution will be discussed. Figure 180 shows the H-field distribution at cross section X = 7.5 mm and at a frequency of 1.09

GHz. The silicon substrate behaves in the slow wave mode and hence the H-field penetrates uniformly through the silicon and the dielectric.

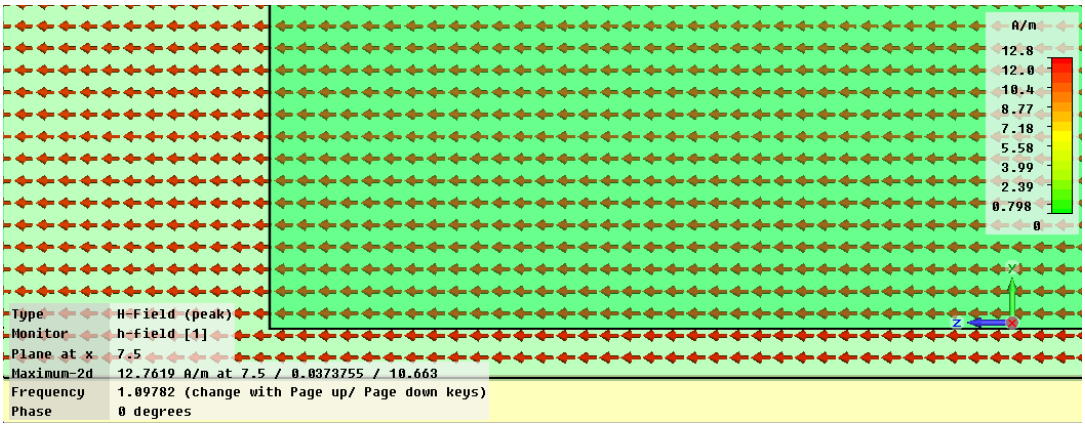


Figure 180 H-field plot at cross section X = 7.5 mm and frequency 1.09 GHz

In Figure 181, the magnetic field distribution is plotted at cross section X = 3.0 mm and at a frequency of 1.09 GHz. Since the cross section is at a region that is outside the embedded silicon, the H-field distribution across the cross section is uniform throughout. As the material in this region is homogenous in nature it is not surprising that the H-fields are also uniform.

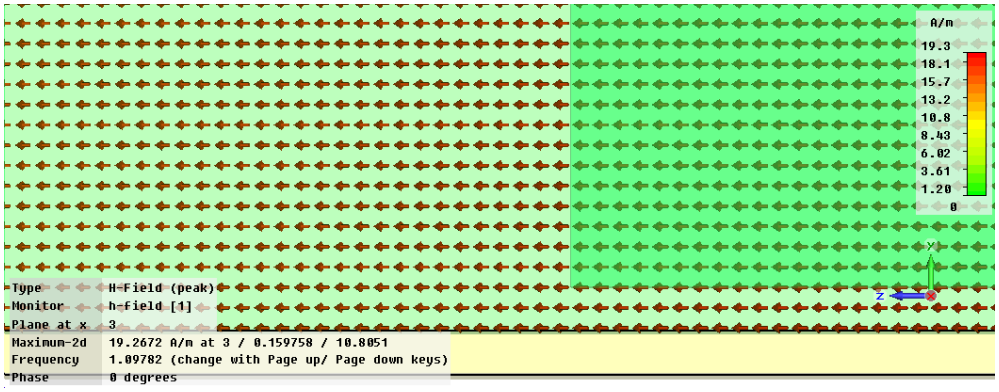


Figure 181 H-field plot at cross section X = 3.0 mm and frequency 1.09 GHz

Figure 182 shows the magnetic field distribution plotted at cross section X = 7.5 mm and at a frequency of 5.0 GHz. As can be seen from the figure, considerable amounts

of magnetic fields penetrate through the silicon substrate, which indicates the existence of slow wave mode until up to 5 GHz.

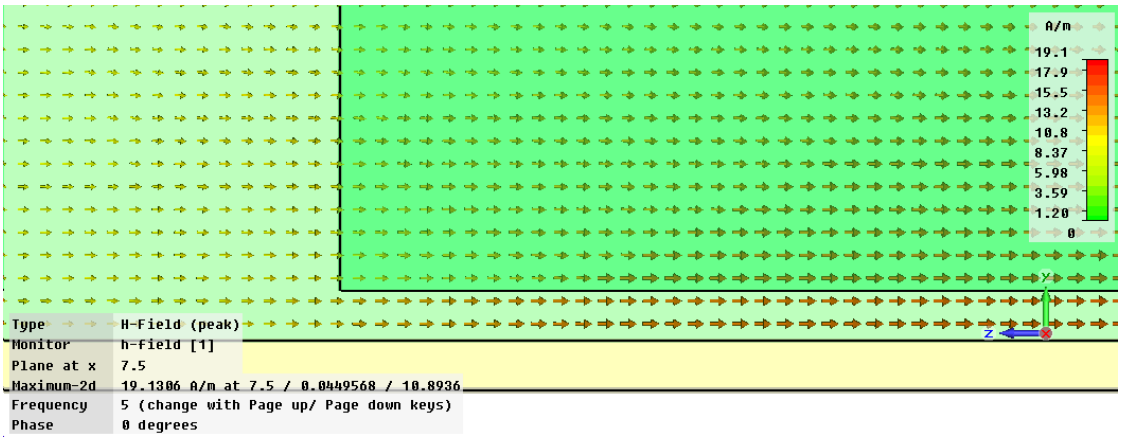


Figure 182 H-field plot at cross section X = 7.5 mm and frequency 5.0 GHz

Figure 183 shows the magnetic field distribution plotted at cross section X = 3.0 mm and at a frequency of 5 GHz. Since the cross section is at a region that is outside the embedded silicon, the H-field distribution across the cross section is uniform throughout.

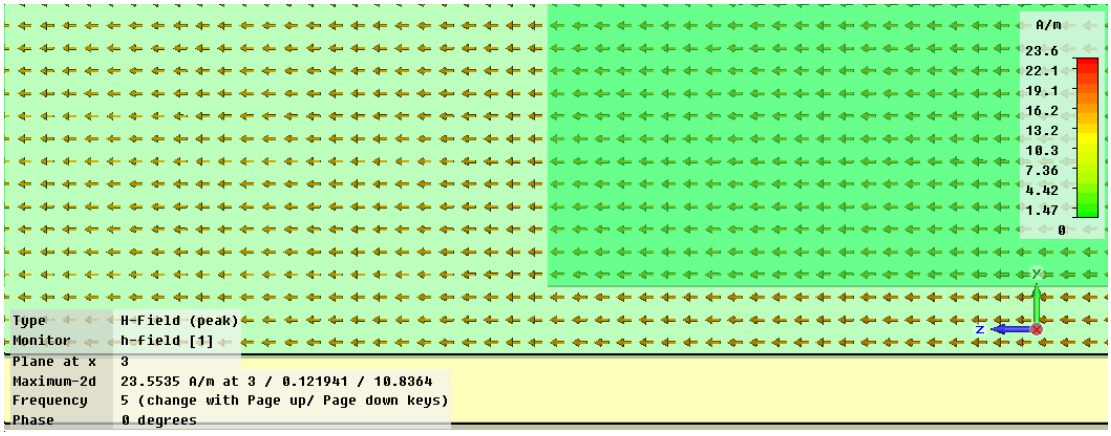


Figure 183 H-field plot at cross section X = 3 mm and frequency 5.0 GHz

6.5.2 1000 S/m Skin Effect mode 7–12GHz

As the frequency increases to over 7 GHz, the silicon substrate starts to transition from slow wave mode to skin effect mode, which is marked by the withdrawal of

magnetic field from the silicon substrate. Figure 184 shows the electric field distribution plotted at cross section X = 7.35 mm and at a frequency of 7 GHz. The E-field vectors are aligned normally to the silicon and dielectric interface, while they are vertically directed in the regions consisting of homogenous dielectric. In the frequency regions up to about 5 GHz, the slow wave mode is distinctly pronounced. Beyond 5 GHz, in the vicinity of the boundary of slow wave mode, the transition to skin effect mode takes place. In the following, the skin effect mode is demonstrated by sampling the E and H-fields at different cross sections and frequencies to demonstrate this transformation.

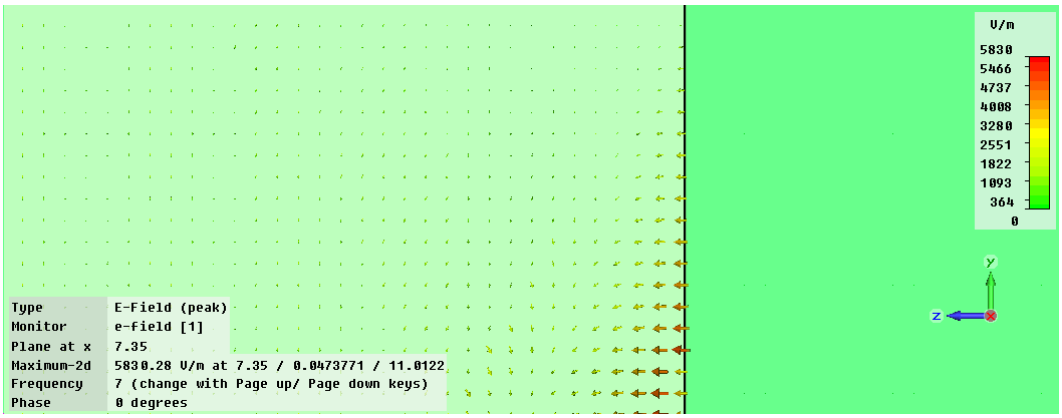


Figure 184 E-field plot at cross section X = 7.35 mm and frequency 7.0 GHz

Another E-field distribution plot at the same cross section as in Figure 184 but at a higher frequency of 11.38 GHz is shown in Figure 185 to show the existence of skin effect mode. The electric field vectors consistently behave as in the case of a metal dielectric interface in the vicinity of edge of embedded silicon substrate and there is almost no penetration of E-field through the silicon substrate.

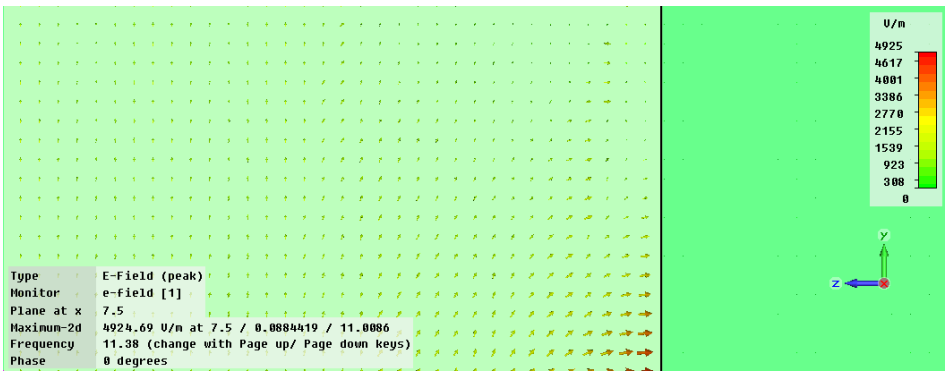


Figure 185 E-field plot at cross section X = 7.5 mm and frequency 11.38 GHz

Figure 186 shows the electric field distribution plotted at cross section X = 3.0 mm and at a frequency of 10.88 GHz. Here since the cross section is at a region that is outside the embedded silicon, the E-field distribution in the homogenous dielectric region is not impacted by the transition from slow wave to skin effect mode of the embedded silicon. In Figure 187 the corresponding H-field distribution is shown for a higher frequency of 12 GHz. A similar behavior is observed in the homogenous dielectric region.

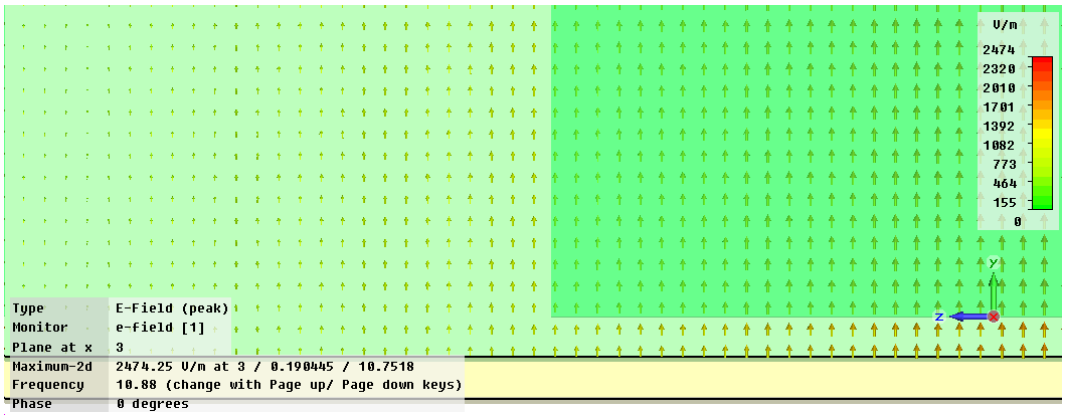


Figure 186 E-field plot at cross section X = 3.0 mm and frequency 10.88 GHz

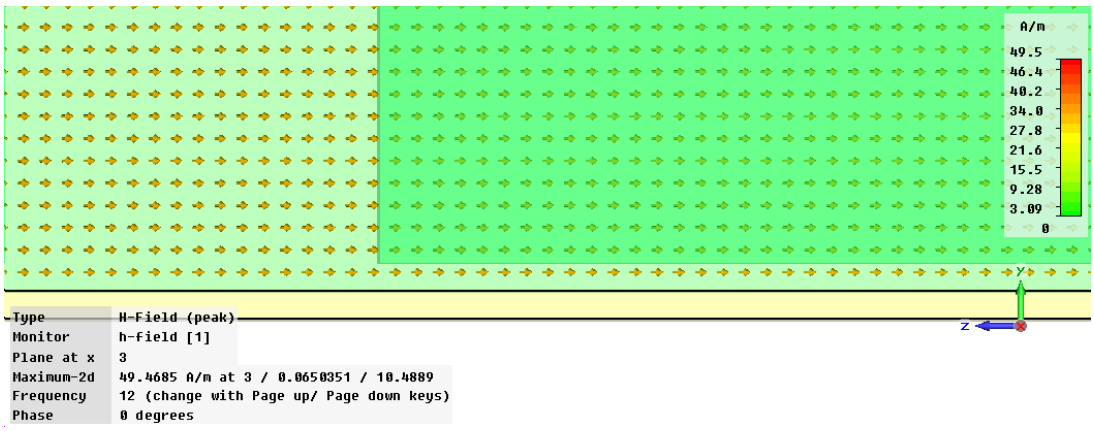


Figure 187 H-field plot at cross section X = 3.0 mm and frequency 12.0 GHz

Now, the magnetic field distribution is considered at the cross sections where the silicon substrate is embedded. Figure 188 shows the magnetic field distribution plotted at cross section X = 7.5 mm and at a frequency of 11.69 GHz. In this figure, the H-field distribution at the interface indicates skin effect mode behavior characterized by the withdrawal of the H-field vectors from the silicon substrate as opposed to freely penetrating through the embedded silicon, which was the case at lower frequencies when the mode was distinctly slow wave. Notice the difference in the behavior of the electric and magnetic fields, which is a clear indication of the slow wave and skin effect modes, and the transition from one to another.

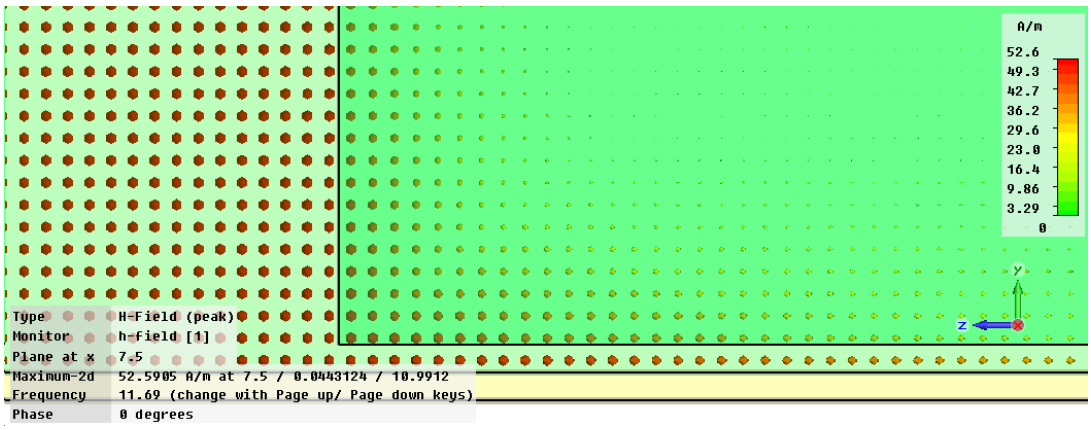


Figure 188 H-field plot at cross section X = 7.5 mm and frequency 11.69 GHz

6.6. Substrate Coupling in Silicon of Very High Conductivity: 6000 S/m

In this section, silicon substrate of conductivity 6000 S/m is considered in the frequency range extending from dc to 12 GHz. The transition from slow wave to skin effect mode is captured by sampling E and H-fields at various frequency points and cross-sections. This case is similar to 1000 S/m conductivity except that the transition happens at a lower frequency.

6.6.1 6000 S/m Slow wave mode up to 5 GHz

Here at a low frequency in the range of hundreds of MHz, slow wave mode is observed. As the frequency increases in to the GHz range, the mode changes to skin effect. Figure 189 shows the electric field distribution plotted at cross section X = 7.5 mm and at a frequency of 100 MHz. As seen in the figure, the E-field vectors are oriented normally to the dielectric silicon interface and there is no penetration of the E-field in to the silicon substrate. Whereas the magnetic field distribution at the same cross section and frequency in Figure 190 shows a uniform penetration of magnetic field through the

silicon substrate and the dielectric surrounding it. This indicates the presence of a slow wave mode in the MHz frequency range.

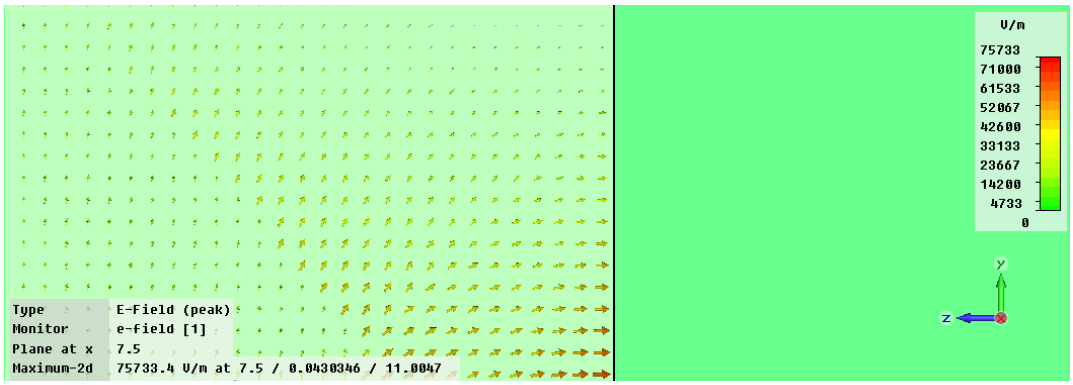


Figure 189 E-field plot at cross section X = 7.5 mm and frequency 100 MHz

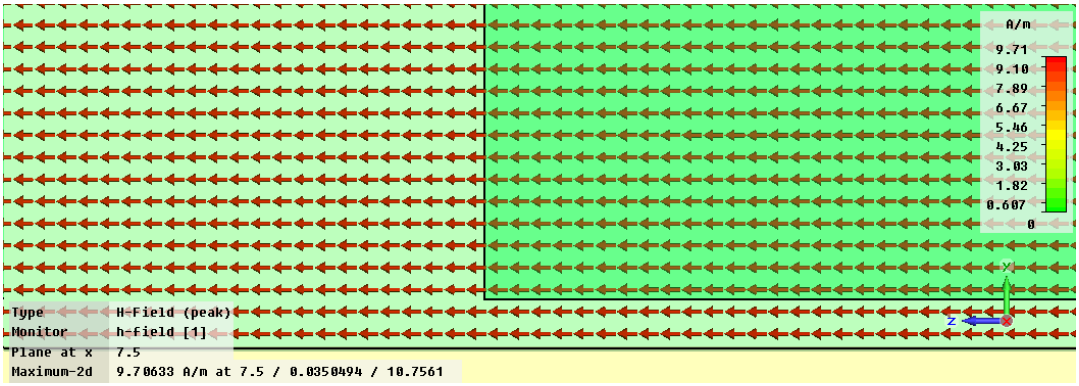


Figure 190 H-field plot at cross section X = 7.5 mm and frequency 100 MHz

As the frequency increases to over 1 GHz as shown in Figure 191, the magnetic field within the embedded silicon starts vanishing indicating the onset of transition from slow wave to skin effect mode. Another field distribution plot at the same cross section as before (shown in Figure 192) but at a higher frequency of over 2.5 GHz shows the progress of transition from slow wave to skin effect mode. Figure 193 shows a cross section at X = 2.85 mm and at a frequency of 2.5 GHz. As this cross section is made outside the region of embedded silicon, the effect of transition is not present at this cross

section, which is manifested by the uniform magnetic field distribution across the cross section.

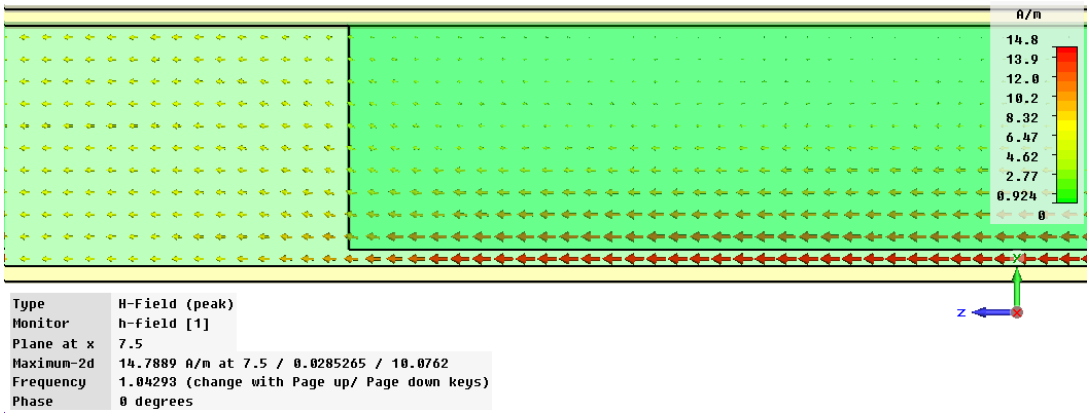


Figure 191 H-field plot at cross section X = 7.5 mm and frequency 1.04 GHz

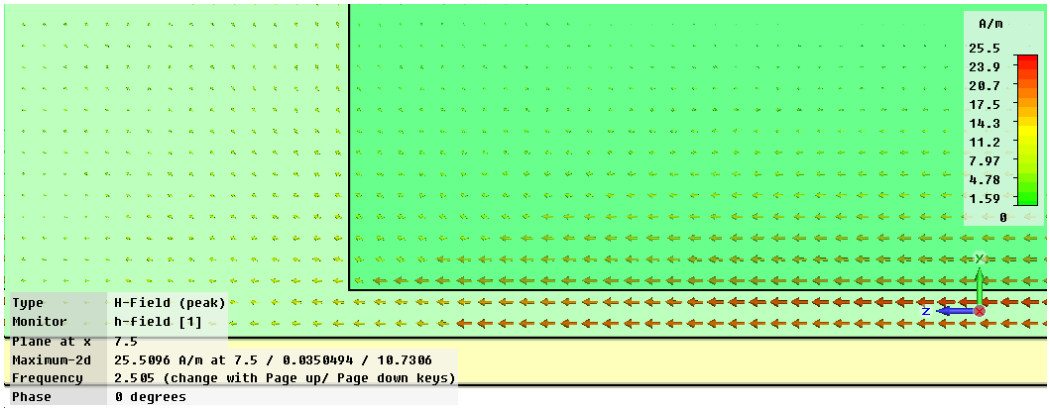


Figure 192 H-field plot at cross section X = 7.5 mm and frequency 2.5 GHz

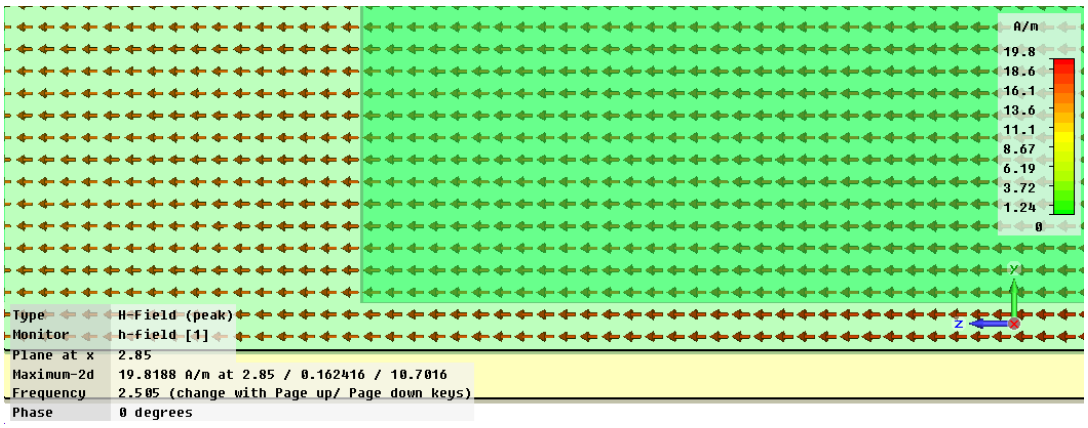


Figure 193 H-field plot at cross section X = 2.85 mm and frequency 2.5 GHz

6.6.2 6000 S/m Skin Effect mode 7–12 GHz

As the frequency increases to over 7 GHz, the skin effect mode becomes more and more pronounced. Figure 194 and Figure 195 show the E-field distribution at cross section X = 7.5 mm and at frequencies 7 and 12 GHz. As seen from the figures, the E-field in the region where the silicon is embedded is primarily concentrated in the dielectric region below the silicon. In Figure 196, a zoomed in version of the E-field at the silicon and dielectric interface is shown, which indicates the silicon is assuming metallic properties, thereby avoiding the penetration of E-field. In contrast, the cross section at X = 2.1 mm and at a frequency of 10.235 GHz in Figure 197, which corresponds to the region where there is no embedded silicon, shows a uniform E-field distribution across the entire cross section.

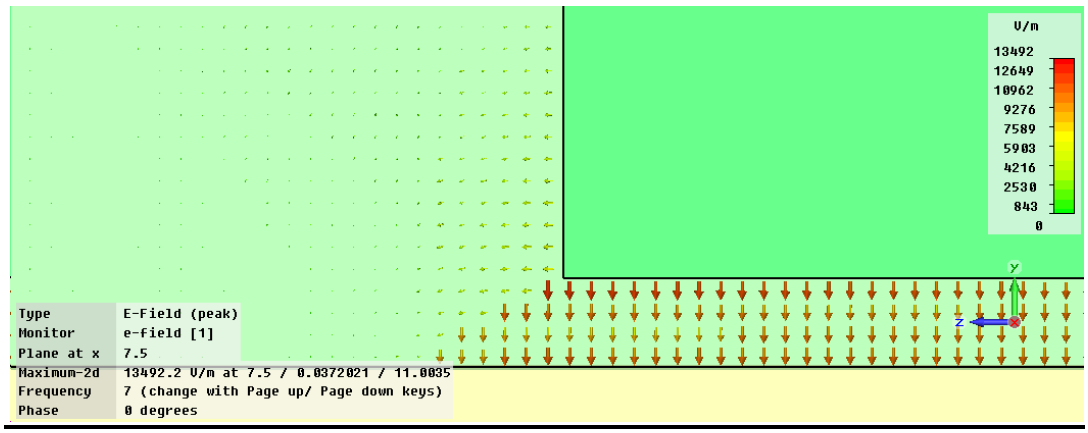


Figure 194 E-field plot at cross section X = 7.5 mm and frequency 7.0 GHz

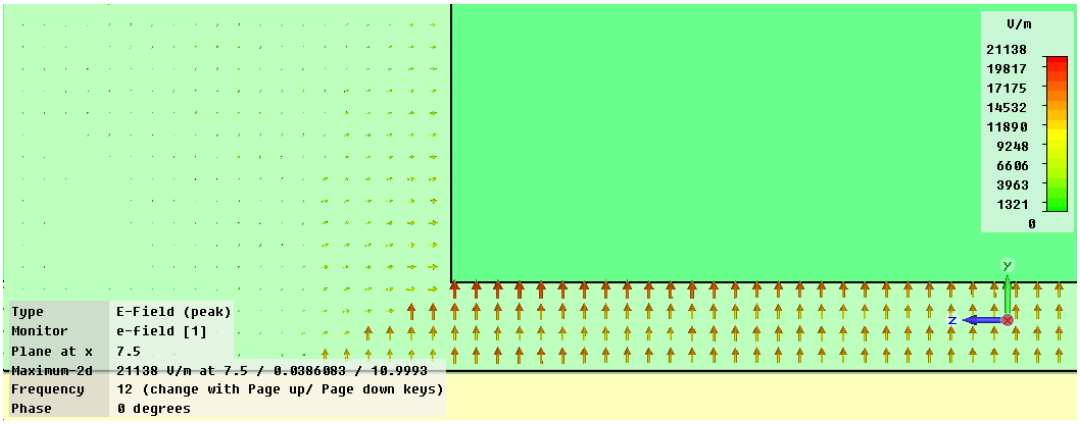


Figure 195 E-field plot at cross section X = 7.5 mm and frequency 12.0 GHz

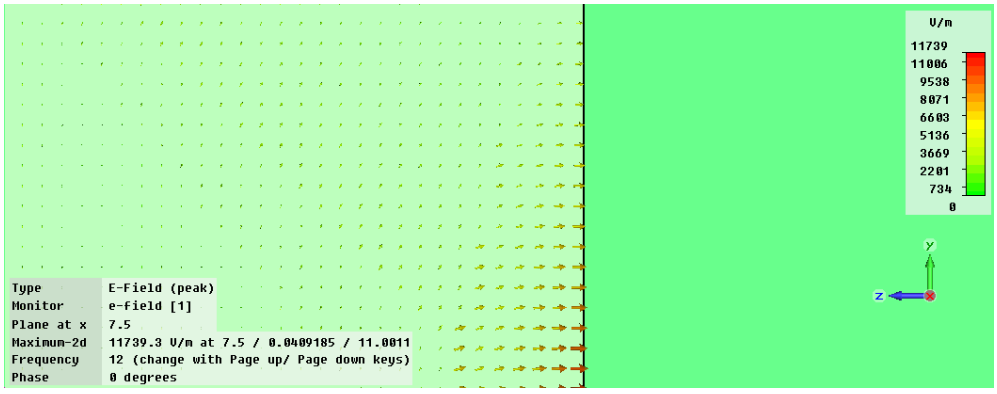


Figure 196 Closer view of E-field distribution in Figure 195 at the interface at X = 7.5 mm and frequency 12.0 GHz

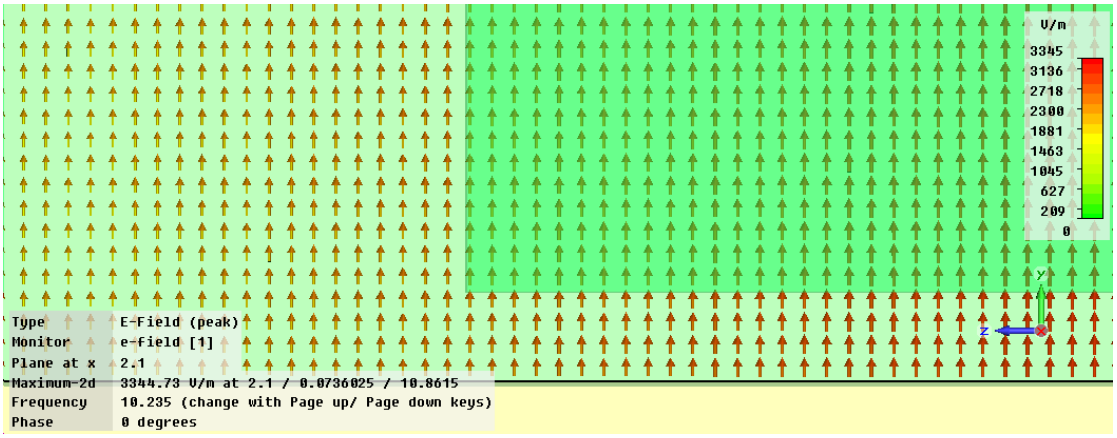


Figure 197 E-field plot at cross section X = 2.1 mm and frequency 10.235 GHz

In Figure 198 and Figure 199, the magnetic field distribution at cross section X = 7.5 mm and frequencies 7 and 12 GHz is shown. It can be seen that as the frequency increases the magnetic field withdraws from the embedded silicon, which indicates that the skin effect is getting more and more pronounced. In contrast the cross section outside the region of embedded silicon as shown in Figure 200, has a uniform magnetic field distribution.

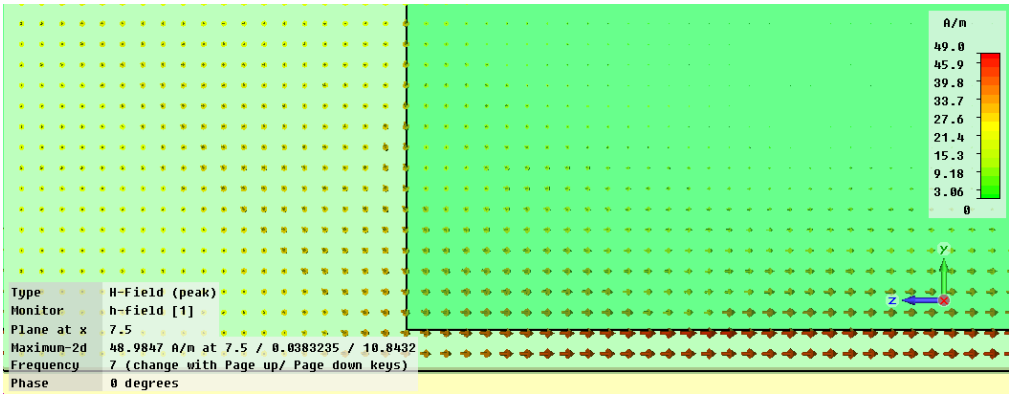


Figure 198 H-field plot at cross section X = 7.5 mm and frequency 7.0 GHz

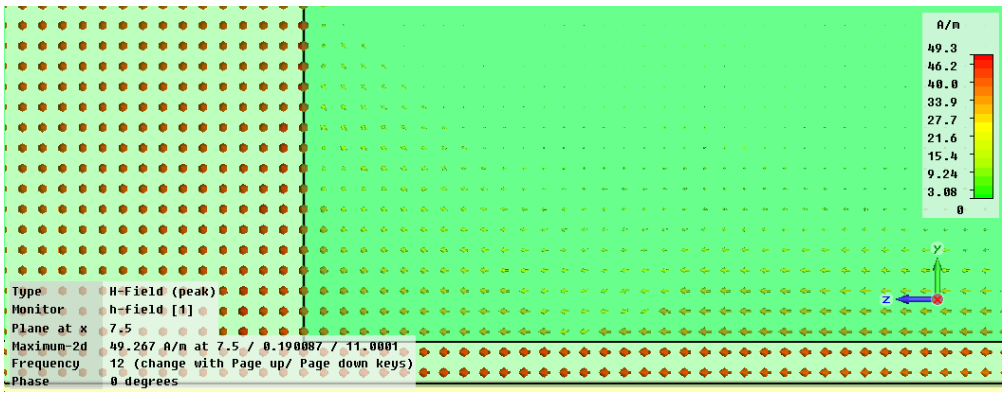


Figure 199 H-field plot at cross section X = 7.5 mm and frequency 12.0 GHz

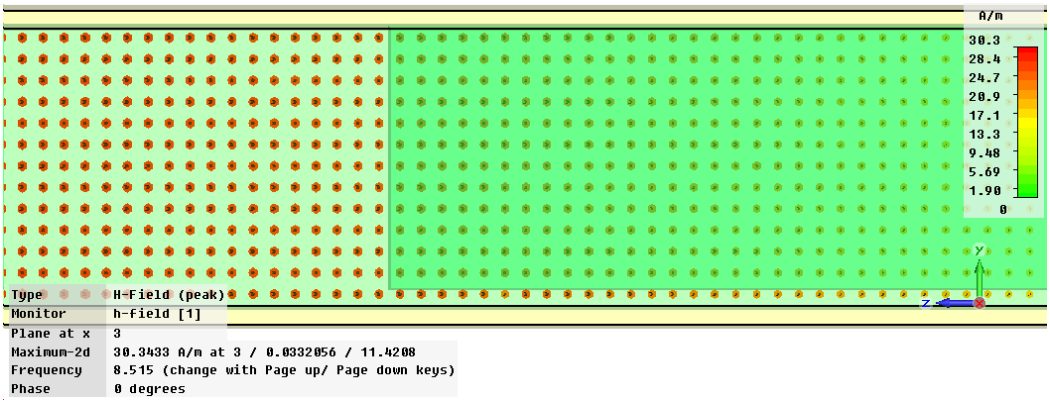


Figure 200 H-field plot at cross section X = 3.0 mm and frequency 8.5 GHz

In Figure 201 below, S parameter transfer responses for the coupling across ports 1 and 2 for the same cross-section as in Figure 157 are shown. The graph shows the results for coupling across the package for the embedded chip with conductivities of 1000 S/m and 6000 S/m. Also, the silicon chip is modeled as a complete metal (copper) to compare the responses with silicon of high conductivity values. The package size is 15 X 15 mm with an embedded chip of size 7 X 7 mm. It can be seen from the results that as the silicon progresses into the skin effect mode, its response becomes similar to that of an embedded block of metal.

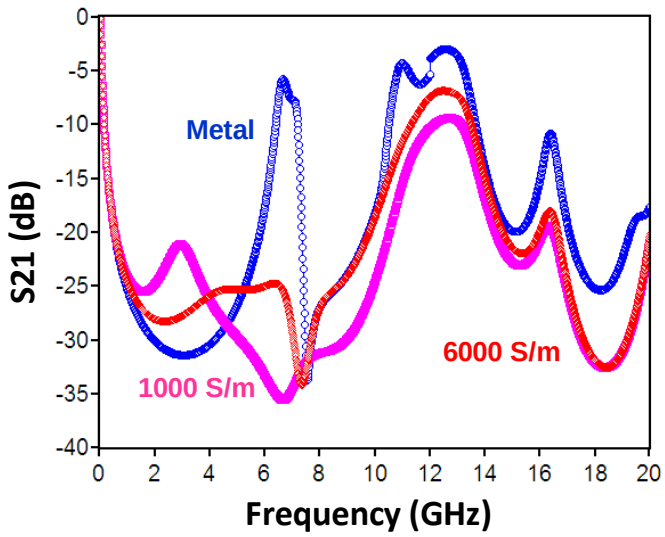


Figure 201 Isolation across the package with embedded silicon of conductivities 1000 S/m and 6000 S/m

6.7. Validation of EM Solver using Measurement Results from On-chip Transmission lines

The results presented so far in this section make extensive use of full wave EM solver. Considering that the behavior exhibited by silicon varies over a broad spectrum of material properties, it is important to ensure that the EM solver can capture this variation in the behavior of silicon appropriately. In this section, a test case involving a micro-strip transmission line on a two layer substrate, consisting of silicon and oxide layers is analyzed. The slow wave factor and the real and imaginary components of characteristic impedances of the transmission line are computed for various silicon resistivities. The results indicate similar behavior as shown in [**130**] and [**135**], where fabricated test vehicles of similar structures have been measured. This gives confidence that the results produced by the EM solver in this section are indeed robust and correct.

The test case used for the simulation in this section consists of a substrate stack-up made up of a silicon layer of thickness 200 um and an oxide layer of thickness 1 um. The permittivity of silicon is 11.8 and that of silicon dioxide is 3.9. The transmission line is 160 um wide. The propagation constant γ and the complex characteristic impedance Z_c are obtained from the simulations. The phase constant β extracted from γ and the real Z_{cr} and imaginary Z_{ci} parts of the complex characteristic impedance Z_c are plotted against various silicon conductivities ranging from 1 to 6000 S/m at a frequency of 0.5 GHz. The results of the simulations are shown in Figure 202, Figure 203, and Figure 204. At the frequency of 0.5 GHz, slow wave mode is exhibited across the conductivity range considered for the simulations. As the conductivity increases, the slow wave factor increases as described in [**130**]. Once the conductivity reaches very high values over 1000 S/m, the slow wave factor starts to reduce because of the transition to skin effect mode. This behavior is demonstrated in Figure 202, which is a plot of silicon conductivity vs. slow wave factor. In Figure 203 and Figure 204, the real Z_{cr} and imaginary Z_{ci} parts for various silicon conductivity values are shown. It is seen that as the conductivity increases while being in the slow wave mode, the real and imaginary parts of the impedance register a monotonic decrease. This behavior is typical of slow wave mode and is characterized experimentally in [**135**].

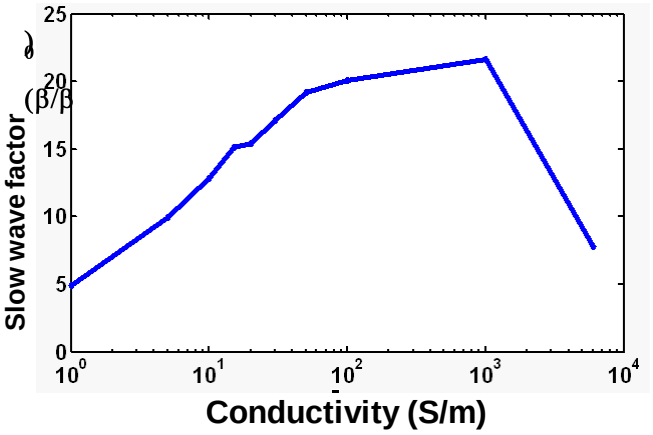


Figure 202 Slow wave factor vs. silicon conductivity

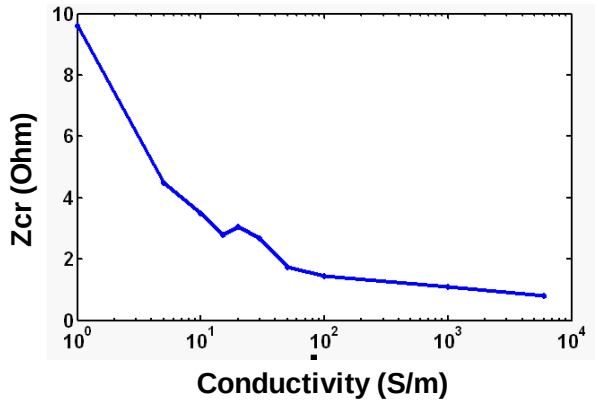


Figure 203 Characteristic impedance Zcr (real part) vs. silicon conductivity

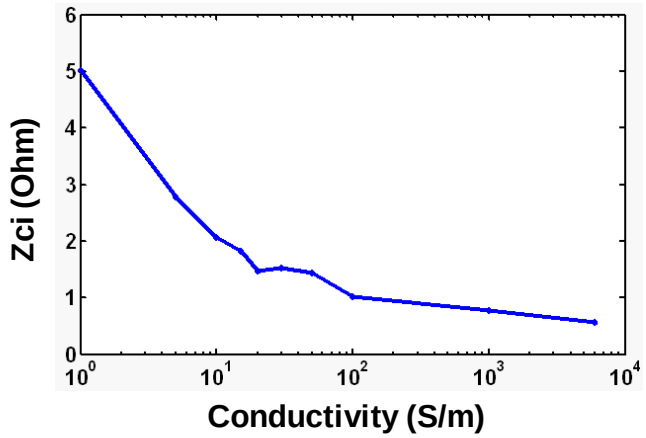


Figure 204 Characteristic impedance Zci (imaginary part) vs. silicon conductivity

6.8. Concluding Remarks

Embedded actives technology targets a wide gamut of applications involving modules with digital, RF/analog chips etc., fabricated using various technologies. Given the diversity of fabrication techniques and their use, embedded chips will consist of silicon substrates of varying resistivities, ranging from 0.02 ohm-cm to 100 ohm-cm. In this chapter, the various modes of propagation exhibited by silicon substrate were analyzed in an embedded environment and the impact of the embedded silicon on the coupling across the package was investigated by considering chips of different resistivities over a frequency range up to 12 GHz. In particular, this chapter focused on scenarios where the cavity within which the chip is embedded has to be covered. The effect of coupling of EM waves from the package with the substrate of the embedded chip for various chip resistivities and build-up layer thicknesses were demonstrated through simulations performed using EM solvers. From a design perspective it is important to understand when the mode transition takes place in order to account for the electric or magnetic fields, or both that enter the bulk substrate of the embedded chip. The parameters that decide this are the thickness of bulk substrate of the embedded chip and the thickness of the build-up layer over which the chip is assembled in the package.

The resonances that occur across the power –ground cavity in the package are influenced by the mode exhibited by the embedded silicon substrate and the lateral dimensions of the chip. The responses show a transition from that of an embedded dielectric block with silicon permittivity to an embedded metal block as the conductivity of the embedded silicon chip is increased. Next, the ratio between the width of the package W and the width of the embedded chip 2a determines if the chip will affect the

package resonances. In particular, it was observed if W/2a is less than 2.5 for silicon of conductivity 1 S/m, the embedded silicon would start affecting the package resonances. If the ratio of W/2a is greater than 2.5, then the embedded silicon has little effect on the package resonances. Similarly, for embedded silicon of conductivity10 S/m, the value of W/2a below which it starts affecting the package resonances was also found to be 2.5. However for silicon of higher conductivities, the value of W/2a below which the silicon substrate starts affecting the package resonances was found to be higher than 2.5. In other words, a smaller silicon substrate will start affecting the package resonances for higher conductivity values of silicon. Finally, the solver results were validated by comparing with measurement results from literature. The results from this chapter show that the presence of silicon embedded within a cavity in the package alters the resonances in the coupling responses across the package. It is therefore important to understand the interaction mechanism when the chip is entirely embedded within the package in order to implement this technology suitably for any system.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

The demands on consumer electronic products to support high functionality at low cost such as computing, communication and multimedia applications with reduced form factor act as driving forces behind packaging technologies such as System on Package (SOP). SOP aims to utilize the best of System on Chip (SOC) and package integration to achieve higher system performance at lower costs as compared to conventional system modules composed of multiple packages assembled on a system board. SOP enhances the functionality of the package by the integration of active and passive components. In the SOP approach, reduction of form factor is the primary motivation behind embedding active and passive components.

This dissertation focused on the chip-last method of embedding chips within cavities in organic substrates and addressed the design of power distribution network for such packages with embedded chips. The challenges associated with electromagnetic coupling in packages when chips are embedded within the substrate layers and the interaction between the embedded chip and its surrounding package were described. Solutions that remedy the noise coupling along with design methodologies for their implementation in multilayer packages were developed. In the following, design guidelines are presented with the goal of providing a fundamental understanding of the issues that need to be dealt with when adopting SOP technology with embedded chips.

Finally, possible extensions to this dissertation are suggested as future work at the end of this chapter.

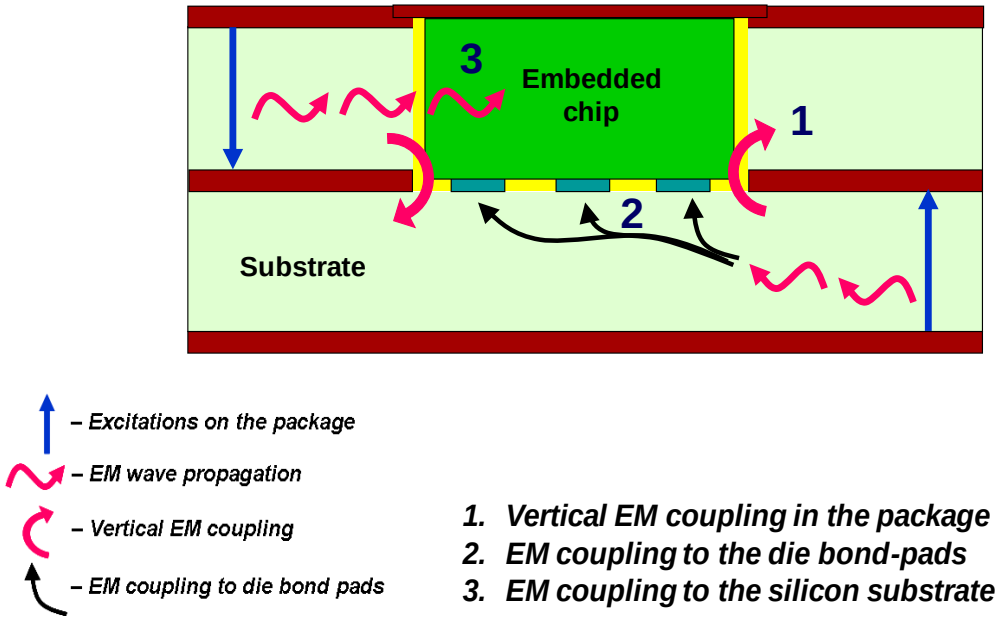


Figure 205 Effects of Electromagnetic Coupling in Packages with Embedded ICs Analyzed in this Dissertation

7.1. Electromagnetic Coupling in Multilayer Packages with Embedded ICs

The first objective of this dissertation is the identification of the electromagnetic effects in multilayer organic packages designed for embedding chips. Chapters 2 – 6 focused on the analysis and demonstration of the challenges to power integrity when chips are embedded within the package. In particular, the figure shown above captures the effects that were dealt with in this dissertation. The following sections summarize the findings of each chapter and discuss the design guidelines for packages with embedded chips based on the findings.

7.1.1 Vertical EM Coupling in Packages with Embedded Chips

Chapter 2 dealt with the noise coupling through the PDN in multilayer packages when apertures are formed on the metal layers and cavities were made in the dielectric layers. The analysis included the effects of parametric variations, such as cavity sizes, apertures on successive metal layers, as well as the presence of dielectric cavities on the noise coupling from one power/ground cavity to another. Some of the findings are listed below:

1. The chip-last method of embedding chip within packages requires cavities causing large apertures in the power/ground planes of the package to accommodate the chips thereby resulting in significant vertical coupling in the package. The apertures formed to embed the chips are much larger as compared to antivia holes or connector slots with the vertical coupling reaching levels of -20dB and even higher.
2. In certain scenarios involving embedded chips, apertures are made on successive plane layers in the package. In these cases, vertical coupling across the multilayer stack-up is caused by the fields fringing from the edges of the apertures. The resonances in the vertical coupling are due to the fringe fields and the parallel plate cavity (formed by the power and ground planes) modes are suppressed.
3. The removal of dielectric material to accommodate the chips does not influence the fringe fields from the aperture edges considerably, provided the location of apertures in the metal layers remain the same. The die to cavity clearance again does not influence the vertical coupling in the

package down to a clearance of 25 um on each side of the embedded chip. A simple model of the package with a homogeneous dielectric with appropriate apertures in the metal layers is a good enough approximation to estimate the frequencies at which high vertical coupling is experienced across the plane pair cavities of the PDN.

7.1.2 EM Coupling on Bond Pads of the Embedded Chip

The influence of current source excitations, setup due to via transitions across the package power – ground planes, on the bond pads of the chip embedded within the substrate cavity was analyzed in Chapter 5. The vias through the plane pair cavities radiate EM waves that get guided through the parallel plate cavity. When the bond pads of the embedded chip are contained within the plane pair cavity, they experience coupling due to EM wave transmission through the power distribution network. The factors that significantly contribute to EM coupling at the bond pads include the configuration of layer stack-up and the proximity of the bond pads to the apertures on power and ground planes that are formed to embed the chip. The EM coupling also manifests itself as noise voltages at the bond pads of embedded chips, which was characterized. The following summarizes the conclusions of Chapter 5:

1. The proximity of aperture edge on the package power and ground planes and the bond pads of the embedded chip impact the coupling to the bond pads significantly. In the case of chips with peripheral bond pad layout, the coupling from the package affects significantly the power and ground pads as

well since they are located close to the cavity edge. This effect is comparatively reduced in the case of array area pad layout with the core power and ground pads located in the centre of the chip.

2. The dielectric thickness of the package is another important factor that determines the magnitude of coupling experienced at the bond pads. Thicker dielectric materials induce voltage fluctuations of larger magnitude at the chip bond pads.
3. The complexity of the analysis of noise coupling at the chip bond pads increases with the number of bond pads in the chip. Considering that a number of chips have hundreds of bond pads (I/Os), and in real packages there could be many aggressor locations which dynamically change under various operating conditions of the chip, it would be very time consuming to accurately estimate the impact on each bond pad. Methods to minimize this challenge are discussed in the following sections.

7.1.3 EM Coupling on the Substrate of Embedded Chip

Certain design scenarios require the cavity within which the chip is embedded to be closed using a grounded plane. These include cases when the back metallization of the embedded chip needs to be grounded, or when a grounded heat spreader (such as a metal sheet or foil) is placed over the cavity for heat dissipation purposes. Under these conditions, the chip substrate can be enclosed within a plane pair cavity formed by power and ground planes, which mean that electromagnetic waves can now couple with the chip substrate. The EM waves injected into the bulk substrate affect the proper working of the

on-chip active and passive components. Therefore, it is important to understand and characterize the EM coupling impacting the chip substrate in order to take preventive measures. The goal of Chapter 6 was to analyze how the embedded silicon IC will interact with the electromagnetic coupling from the package.

Following is the summary of the analyses from Chapter 6:

1. The substrate of the embedded silicon chip exhibits different modes such as slow wave, quasi-dielectric and skin effect depending on the ratio of thicknesses of the silicon chip and the build-up layer below, the frequency of operation and resistivity of the silicon substrate.
2. The mode exhibited by the silicon substrate determines the penetration of electric and magnetic fields through the substrate which in turn affects the on-chip active and passive circuits. Low resistivity silicon substrate (~0.1 mOhm) where the bulk behaves predominantly in skin effect mode (assumes metallic properties) is immune to the impact of EM coupling from the package.
3. In the case of medium and high resistivity silicon substrates, either magnetic or both electric and magnetic fields (slow wave and quasi dielectric modes respectively) set-up in the package penetrate the substrate and on-chip circuits need to be analyzed for the impact of this coupling.
4. The parallel plate resonances in the plane pair cavity formed by the power and ground planes housing the embedded chip are suppressed. This is because of the increased loss offered by silicon as compared to dielectric materials.

5. The thickness of the build-up layer supporting the embedded chip and the size of the embedded silicon substrate play an important role in making the influence of embedded silicon felt on the resonances in EM coupling. As the thickness of the dielectric build-up layers below the embedded silicon substrate increases, approaching the thickness of embedded silicon, the effect of the embedded chip on the coupling across the package reduces.
6. The following are the factors which influence the resonances of parallel plate cavities in the PDN of the package in descending order of importance
    a. Resistivity of the embedded chip's substrate
    b. Lateral dimensions of the embedded chip
    c. Thickness of the build-up layer over which the chip is assembled inside the cavity within the package
    d. Permittivity of the dielectric material used for build-up layer below the embedded chip

7.1.4 Suppression of Electromagnetic Coupling on Embedded Chip

The previous sections discussed the various effects of electromagnetic coupling in packages with embedded chips. In this section, ways to minimize and tackle the coupling of EM waves with the embedded chip are discussed. The solutions proposed address the challenges associated with electromagnetic coupling as shown in Figure 205.

7.1.4.1 Modification of Layer Stack-up

The setup in this section is a four metal layer package, such that one layer is used for power, one for ground, one for chip fan out and a final one for Ball Grid Array (BGA) pads of the package. Here the back metallization of the chip does not require grounding. Using the following cases, simple design guidelines are presented for identifying cases where the coupling from the package could significantly affect the chip.

Case 1. The chip is embedded in such a way that the ground and power layers sandwich the fan out layer as shown in Figure 206. In this case, as explained in Chapter 4 the impact of EM waves setup in the parallel plate cavity formed by the power/ground planes on the bond pads could potentially be severe. The impact manifests itself as voltage fluctuations at the chip bond pads, which could affect the proper functioning of the embedded chip.

The layer stack-up in Case 1 is modified such that the power and ground planes do not sandwich the fan out layer. This rearrangement is illustrated in Figure 207. Since the fan out layer is outside of the plane pair cavity, the signal lines that are routed will have a good reference though the bond pads can still experience coupling due to fringing fields from the aperture edges on the planes. This helps to minimize the overall voltage fluctuations experienced by the bond pads along the route from the chip to the package BGAs. Also, under this arrangement, the power – ground cavity has more clearance to implement EM coupling suppression

schemes such as decoupling capacitors. The drawback of this setup is that the thickness of the dielectric materials as well as the arrangement of build-up and core layers in the layer stack-up may have to be changed to accommodate the modification.

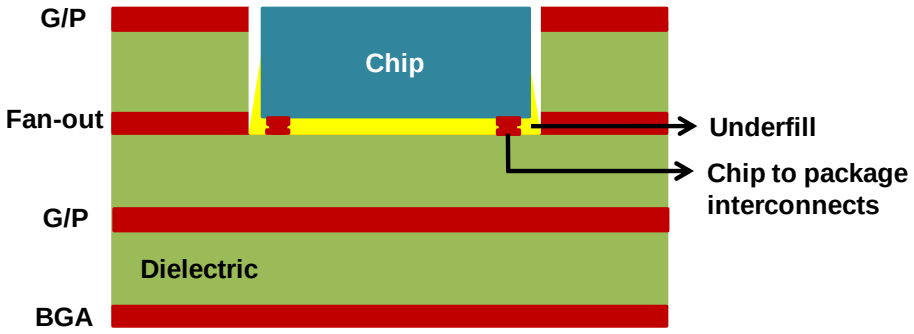


Figure 206 Multilayer package and its interconnection to embedded chip

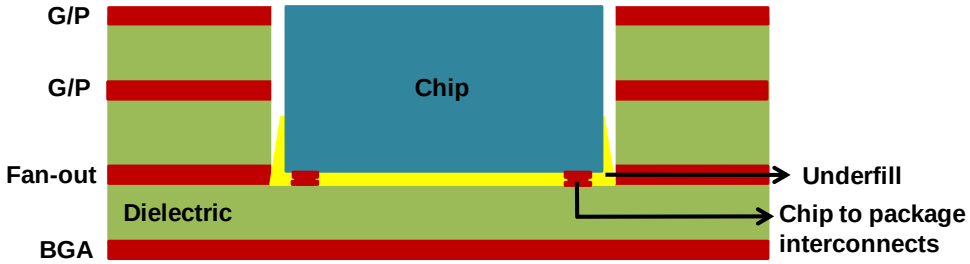


Figure 207 Multilayer Package in Figure 206 with modified layer stack-up

Case 2. If the package consists of multiple pairs of power (possibly of different voltages) and ground planes as shown in Figure 208, this could lead to a case similar to Case 1, where the fan out of the embedded chip is contained within a single pair of power and ground planes. To remedy the situation, the layer stack-up can be modified as discussed below.

In this case, the layer stack-up of the multilayer package shown in Figure 208 is modified to facilitate embedding the chip. Figure 209 shows the modified layer stack-up that can help minimize the impact of EM coupling at the bond pads. The modification is made by rearranging the power and ground planes such that the fan out layer of the chip is not contained within any parallel plate cavity constituted by planes of opposing polarity. In general, the rearrangement should lead to parallel plate cavities that are completely above or below the fan out layer of the chip. This method of rearranging layers in the multi layer stack-up is similar to Case 1, except that it has been extended to packages with multiple pairs of power and ground planes.

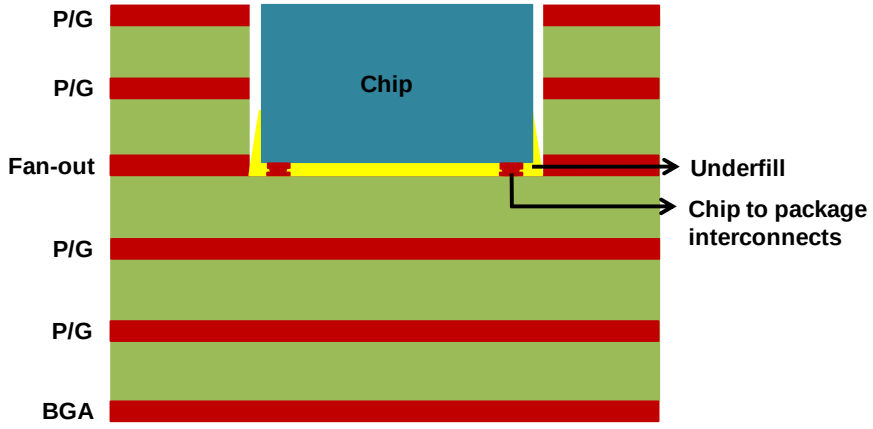


Figure 208 Multilayer package with multiple power/ground plane pairs and embedded chip

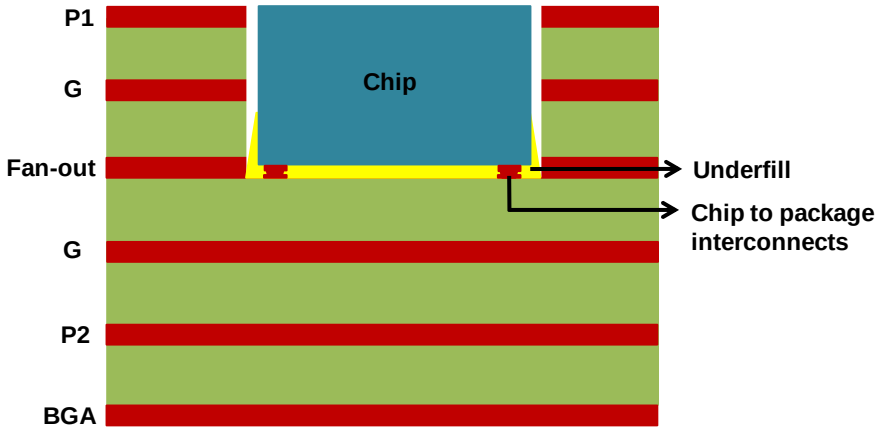


Figure 209 Modified layer stack-up for the package in Figure 208

In some cases, the rearrangement can lead to having a power layer on the exterior. Also, there may be situations listed in the following section where modifying the layer stack-up may not provide a solution. The following section discusses the solution for these circumstances.

7.1.4.2 Coupling Suppression using EBGs

Case 3. Consider the following scenarios:

a. Same as Case 1 except that the modification of layer stack-up is not possible

b. The back metallization of the chip needs to be grounded thereby enclosing the chip within the package

c. When it is not possible to drill a cavity extending across multiple build-up/core dielectric layers.

In the above situations, patterning a power plane that contains the aperture for embed a chip suitably with EBGs, as explained in Chapter 3, will help mitigate the problem of electromagnetic coupling affecting the embedded chip. Chapter 3 discussed the suppression of EM wave propagation using EBGs across multiple power – ground parallel plate cavities. Chapter 4 discussed the synthesis of EBGs for a given input band gap frequency specification and also a dispersion diagram based methodology for implementing the synthesized EBGs in a multilayer stack-up with apertures to embed a chip.

7.2. Future work

SOP technology with embedded actives holds enormous promise for the future of semiconductor industry, and has the potential to bring about substantial reduction in form factor as well as integration of multiple functionalities. However, before this technology is ready for the real world, a few technological challenges have to be overcome. The main contribution of this dissertation is the identification of the challenges associated with electromagnetic interference in packages with embedded chips as well as methods to overcome the problems faced. Although the dissertation has identified, analyzed and quantified some of the predominant issues that arise with respect to chip-package interaction, there are possible venues for future work, which are discussed below.

1. Analysis of chip package interaction carried out in this dissertation mostly involved test vehicles assembled with dummy chips consisting of daisy chain structures on a single metallization layer. The reason for using this simple setup was to ensure that the chip complexity did not interfere with

the understanding of the phenomena. If this technology is to be adopted commercially, additional studies will have to be conducted with a real functional embedded chip to gain an even better understanding of the chip and package interaction mechanisms.

2. Electromagnetic coupling to the substrate of the embedded chip was analyzed with chips whose substrates were biased to ground. However, in some cases, the substrate is biased to a non-zero voltage. The effect of non-zero substrate bias for an embedded chip package is an interesting area for further study.
3. The dispersion diagram based band gap prediction methodology for multilayer EBG structures used a multilayer unit cell containing the aperture. The coupling through the aperture in the unit cell was estimated using an EM solver. So far the coupling through apertures in multilayer packages has been analyzed for slots and slits, where one of the lateral dimensions is assumed to be infinite. In the case of apertures made to embed chips, the electromagnetic fields along both lateral dimensions need to be analyzed (by not assuming either of the lateral dimensions to be infinite) for a numerical evaluation of the coupling through the aperture, which is a possible area of future work.

7.3. Papers Published

The following papers were published as part of this dissertation.

7.3.1 Journal Papers

[1] Bharath, K; **Sankaran, N;** Swaminathan, M; Tummala, R, **"**Multi-Layer Fringe-Field Augmentations for the Efficient Modeling of Package Power Planes", Accepted to *IEEE Trans. on Adv. Packaging*

[2] **Sankaran, N;** Huh, S; Min, S; Swaminathan, M; Tummala, R, "Suppression of Vertical Electromagnetic Coupling in Multilayer Packages", final review in *IEEE Trans. on Adv. Packaging*

[3] **Sankaran, N;** Swaminathan, M; Tummala, R, "Synthesis methodology for Electromagnetic Band Gap Structures Using Stepped Impedance Resonators", submitted for review in *Microwave and Optical Technology Letters*.

[4] **Sankaran, N;** Chan, H; Swaminathan, M; Sundaram, V; Tummala, R, "Electromagnetic Coupling to Bond pads of Embedded Chips in Multilayer Packages", to be submitted for review in *IEEE Trans. on Electron Devices*.

[5] **Sankaran, N;** Kumbhat, N; Swaminathan, M; Sundaram, V; Tummala, R., "Electromagnetic Coupling to the Chip Substrate of Embedded Chips in Multilayer Packages", to be submitted for review in *Journal of Applied Physics.*

7.3.2 Conference Papers

[1] **Sankaran, N**; Chan, H; Swaminathan, M; Sundaram, V; Tummala, R, "Chip-Package Electrical Interaction in Organic Packages with Embedded Actives", *60th Electronic Components and Technology Conference (ECTC 2011),* Lake Buena Vista, FL, June 2010. Accepted for Publication.

[2] Tummala, R; Sundaram, V; Kumbhat, N**; Sankaran, N**, "Chip-last Interconnection to Thin Organic Packages with Advanced Dielectrics and Fine Pitch I/Os", *2010 Pan Pacific Microelectronics Symposium & Tabletop Exhibition*, Hawaii, pp. 26–28 Jan. 2010.

[3] **Sankaran, N**.; Swaminathan, M.; Tummala, R., "A novel method for suppression of vertical coupling in multi-layered substrates," *Electrical Design of Advanced Packaging and Systems Symposium (EDAPS 2008),* pp.124–127, Seoul, South Korea, December 2008

[4] **Sankaran, N**.; Huh, S.; Swaminathan, M.; Tummala, R., "Suppression of

vertical coupling using Electromagnetic Band Gap structures," *Electrical Performance of Electronic Packaging (EPEP 2008)*, pp.173–176, San Jose, CA, October 2008.

[5] Bharath, K.; **Sankaran, N**.; Engin, A.E.; Swaminathan, M., "Multi-layer fringe-field augmentations for the efficient modeling of package power planes," *Electrical Performance of Electronic Packaging (EPEP 2008)* , pp.331–334, San Jose, October 2008

[6] **Sankaran, N**.; Ramdas, V.C.; Baik-Woo Lee; Sundaram, V.; Ege Engin; Iyer, M.; Swaminathan, M.; Tummala, R., "Coupling noise analysis and high frequency design optimization of power/ground plane stack-up in embedded chip substrate cavities," *58th Electronic Components and Technology Conference (ECTC 2008)*, pp.1874–1879, Orlando, FL, May 2008.

[7] **Sankaran, N**.; Baik-Woo Lee; Sundaram, V.; Engin, E.; Iyer, M.; Swaminathan, M.; Tummala, R., "Electrical Characterization and Design Optimization of Embedded Chip in Substrate Cavities," *57th Electronic Components and Technology Conference (ECTC 2007),* pp.992–999, Reno, NV, May 2007.

7.3.3 Awards

- TI Women's Leadership Fellowship (Aug 2009 – Dec 2010)

- *Best paper award at IEEE Electrical Performance of Electronic Packaging (EPEP 2008)* for paper titled – "Multi-Layer Fringe-Field Augmentations for the Efficient Modeling of Package Power Planes" (Co-author)

REFERENCES

[1] R. Tummala, V. Sundaram, N. Kumbhat, and N. Sankaran, "Chip-last Interconnection to Thin Organic Packages with Advanced Dielectrics and Fine Pitch I/Os," in *Pan Pacific Microelectronics Symposium & Tabletop Exhibition*, Hawaii, USA, 2010, p. 26–28.

[2] S. K. Lim, "Physical design for 3D system on package," *Design & Test of Computers, IEEE*, vol. 22, no. 6, pp. 532--539, Nov. 2005.

[3] T. Kamgaing, et al., "Future package technologies for wireless communication systems," *Intel Technology Journal*, vol. 9, no. 4, pp. 353--364, Nov. 2005.

[4] L. Larson and D. Jessie, "Advances in RF packaging technologies for next-generation wireless communications applications [RFIC]," in *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC 2003)*, San Jose, CA, 2003, pp. 323--330.

[5] E. Mounier. (2007, Jul.) Market trends for 3D stacking. [Online]. http://www.globalsmt.net/documents/Technical_Articles/7.7_mounier.pdf (Feb 20th, 2010)

[6] H. Richter, D. Ferling, F. Buchali, and W. Heck, "Substrate integrated packaging for RF-applications," *Microelectronics International*, vol. 17, no. 1, pp. 31--35, Jan. 2000.

[7] D. Carey. (2008, Oct.) High-Density Packaging Trends in Portable Electronics (2008 CTEA Electronics Design & Manufacturing Symposium). [Online]. http://www.portelligent.com/TechPerspectives/High-Density_Packaging_Trends_in_Portable_Electronics.aspx (Nov 5th, 2010)

[8] R. Tummala, et al., "High density packaging in 2010 and beyond," in *Proceedings of the 4th International Symposium on Electronic Materials and Packaging*, Kaohsiung, Taiwan, 2002, pp. 30--36.

[9] K. Greene. (2009, Feb.) Intel's New Breed of Chips - The chip maker tries to diversify with system-on-chip designs. [Online]. http://www.technologyreview.com/computing/22068/ (Nov 8th, 2010)

[10] K. B. Unchwaniwala, M. F. Caggiano, and R. C. Frye, "Noise generation, propagation and effects on RF components in system-on-a-chip packaging," *Microelectronics Journal*, vol. 33, no. 5-6, pp. 471--478, May 2002.

[11] M. Alexander. (2002, Aug.) Power distribution system (PDS) design: Using bypass/decoupling capacitors. XAPP623 (v. 1.0).

[12] G. Troster, "Potentials of chip-package co-design for high-speed digital applications," in *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, Munich, Germany, 1999, pp. 423-424.

[13] L. .-R. Zheng, H. Tenhunen, and R. Weerasekara. (2008, Apr.) Performance and cost trade-offs for SoC, SoP and 3-D integration (ISSCC Workshop). [Online]. http://www.ict.kth.se/courses/IL2211/IL2211_files/Lecture4_isscc.pdf (Oct 17th, 2010)

[14] Y. Wu and A. Ivanov, "Low Power SoC Memory BIST," in *21st IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT 2006)*, Arlington, VA, 2006, pp. 197-205.

[15] S. Decoutere, G. Carchon, M. Dehan, and A. Mercha, "Passive on-chip components: Trends and challenges for RF applications," *Microelectronic Engineering*, vol. 82, no. 3-4, pp. 503-513, Dec. 2005.

[16] X. Duo, L. .-R. Zheng, M. Ismail, and H. Tenhunen, "On-chip versus off-chip passives analysis in radio and mixed-signal system-on-package design," in *Proceeding of the Sixth IEEE CPMT Conference on High Density Microsystem Design and Packaging and Component Failure Analysis, 2004. HDP '04.*, Hong Kong, China, 2004, pp. 109-116.

[17] L. .-R. Zheng, X. Duo, M. Shen, W. Michielsen, and H. Tenhunen, "Cost and performance tradeoff analysis in radio and mixed-signal system-on-package design," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 364--375, May 2004.

[18] R. Tummala, "SOP: what is it and why? A new microsystem-integration technology paradigm-Moore's law for system integration of miniaturized convergent systems of the next decade," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 241--249, May 2004.

[19] A. Fontanelli, "System-in-Package Technology: Opportunities and Challenges," in *9th International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, 2008, pp. 589--593.

[20] N. Khan, et al., "Development of 3D silicon module with TSV for system in packaging," in *58th Electronic Components and Technology Conference (ECTC 2008)*, Lake Buena Vista, FL, 2008, pp. 550-555.

[21] J. U. Knickerbocker, et al., "3D silicon integration," in *58th Electronic Components and Technology Conference (ECTC 2008)*, Lake Buena Vista, FL, 2008, pp. 538--543.

[22] R. Tummala, "Moore's law meets its match (system-on-package)," *IEEE Spectrum*, vol. 43, no. 6, pp. 44--49, Jun. 2006.

[23] R. Tummala and V. K. Madisetti, "System on chip or system on package?," *IEEE Design & Test of Computers*, vol. 16, no. 2, pp. 48--56, Apr. 1999.

[24] R. Tummala and J. Laskar, "Gigabit wireless: system-on-a-package technology," *Proceedings of the IEEE*, vol. 92, no. 2, pp. 376--387, Feb. 2004.

[25] R. Tummala, et al., "The SOP for miniaturized, mixed-signal computing, communication, and consumer systems of the next decade," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 250--267, May 2004.

[26] N. Sankaran, et al., "Electrical Characterization and Design Optimization of Embedded Chip in Substrate Cavities," in *57th Electronic Components and Technology (ECTC 2007) Conference*, Reno, NV, 2007, pp. 992--999.

[27] W. Daum, W. E. Burdick, and R. A. Fillion, "Overlay high-density interconnect: a chips-first multichip module," *Computer*, vol. 26, no. 4, pp. 23--29, Apr. 1993.

[28] S. N. Towle, H. Braunisch, C. Hu, R. D. Emery, and G. J. Vandentop, "Bumpless build-up layer packaging," in *International Mechanical Engineering Congress and Exposition (ASME 2002)*, New Orleans, LA, 2002, pp. 11--16.

[29] M. Sunohara, K. Murayama, M. Higashi, and M. Shimizu, "Development of interconnect technologies for embedded organic packages," in *53rd Electronic Components and Technology (ECTC 2003) Conference*, New Orleans, LA, 2003, pp. 1484--1489.

[30] A. Ostmann, et al., "Realization of a stackable package using chip in polymer technology," in *2nd International IEEE Conference on Polymers and Adhesives in Microelectronics and Photonics (POLYTRONIC 2002)*, Zalaegerszeg, Hungary, 2002, pp. 160--164.

[31] B. .-W. Lee, et al., "Chip-last Embedded Active for System-On-Package (SOP)," in *57th Electronic Components and Technology Conference (ECTC 2007)*, Reno, NV, 2007, pp. 292--298.

[32] F. Liu, et al., "Chip-last embedded actives and passives in thin organic package for 1–110 GHz multi-band applications," in *Proceedings of the 60th Electronic Components*

and Technology Conference (ECTC) 2010, Las Vegas, NV, 2010, pp. 758-763.

[33] A. Choudhury, et al., "Low temperature, low profile, ultra-fine pitch copper-to-copper chip-last embedded-active interconnection technology," in *Proceedings of the 60th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, 2010, pp. 350-356.

[34] N. Kumbhat, et al., "Highly-reliable, 30µm pitch copper interconnects using nano-ACF/NCF," in *Proceedings of the 59th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, 2009, pp. 1479-485.

[35] K. L. Tai. (2000, Jan.) System-In-Package (SIP): challenges and opportunities. Proceedings of the ASP-DAC 2000 Asia and South Pacific.

[36] F. Carson. Advanced 3D Packaging and Interconnect. [Online]. http://www.kns.com/UPLOADFILES/DGALLERY/CHIPPAC.PDF (Oct 10th, 2010)

[37] E. Bantog, S. Chiu, C. T. Chen, H. P. Pu, and C. S. Hsiao, "Wire bond, flip-chip, and chip-scale-package solution to high silicon integration," in *Proceedings of the 56th Electronic Components and Technology Conference (ECTC)*, San Diego, CA , Jun. 2006, pp. 1--6.

[38] L. Zu, et al., "Improving Microprocessor Performance With Flip Chip Package Designs," in *Proceedings of IEEE Symposium on IC/Package Design Integration, 1998*, Santa Cruz, CA, Feb. 1998, pp. 82-87.

[39] J. J. Lee. (2001, Apr.) Lower costs, technical advantages drive flip-chip technology toward mainstream applications. [Online]. http://www.aseglobal.com/img/event/Flip-Chip%20article%20final_05.01.pdf (June 7th, 2010)

[40] P. Elenius and L. Levine. (2000, Jul.) Comparing Flip-Chip and Wire-Bond Interconnection Technologies. [Online]. http://processsolutionsconsulting.com/pdf/Flip_Bump/csr-7-00.pdf (Feb 7th, 2010)

[41] S. Lin and N. Chang, "Challenges in power-ground integrity," in *IEEE/ACM International Conference on Computer Aided Design (ICCAD 2001)*, San Jose, CA, 2001, pp. 651--654.

[42] J. Kim, et al., "Analysis of noise coupling from a power distribution network to signal traces in high-speed multilayer printed circuit boards," *IEEE Transactions on Electromagnetic Compatibility*, vol. 48, no. 2, pp. 319--330, May 2006.

[43] J. Li, L. Wan, W. Gao, and C. Liao, "Improvement of power integrity with novel segmented power bus structures in RF/digital SOP," in *International Conference on*

Electronic Packaging Technology & High Density Packaging (ICEP-HDP 2008), Shanghai, China, 2008, pp. 1-4.

[44] N. Nenadovic, E. Miersch, M. Versleijen, and S. Wane, "Application of Integral Analysis Technique to Determine Signal- and Power Integrity of Advanced Packages," in *IEEE Electrical Performance of Electronic Packaging Conference (EPEP 2007)*, Atlanta, GA, 2007, pp. 183--186.

[45] D. Rossi, P. Angelini, C. Metra, G. Campardo, and G. P. Vanalli, "Risks for Signal Integrity in System in Package and Possible Remedies," in *13th Test European Symposium*, Verbania, Italy, 2008, pp. 165--170.

[46] S. .-B. Lee, J. Park, S. .-J. Hong, and H. .-G. Jeon, "Electromagnetic interference (EMI) behavior of system in package (SIP)," in *International Symposium on Electromagnetic Compatibility (EMC 2004)*, vol. 3, Notre Dame, IN, 2004, pp. 876--880vol3.

[47] C. Trigas, "Design challenges for system-in-package vs system-on-chip," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, San Jose, CA, 2003, pp. 663--666.

[48] J. Miettinen, M. Mantysalo, K. Kaija, and E. O. Ristolainen, "System design issues for 3D system-in-package (SiP)," in *54th Electronic Components and Technology (ECTC 2004) Conference*, vol. 1, LAs Vegas, NV, 2004, pp. 610--615Vol1.

[49] W. Koh, "System in package (SiP) technology applications," in *6th International Conference on Electronic Packaging Technology (ICEPT)*, Shenzhen, China, 2005, pp. 61--66.

[50] T. Sudo, H. Sasaki, N. Masuda, and J. L. Drewniak, "Electromagnetic interference (EMI) of system-on-package (SOP)," *IEEE Transactions on Advanced Packaging*, vol. 27, no. 2, pp. 304--314, May 2004.

[51] L. Smith and H. Shi, "FPGA design for Signal and Power Integrity," in *DesignCon 2007*, Santa Clara, CA, 2007.

[52] J. .-H. Kim and M. Swaminathan, "Modeling of multilayered power distribution planes using transmission matrix method," *IEEE Transactions on Advanced Packaging*, vol. 25, no. 2, pp. 189--199, May 2002.

[53] J. Choi, et al., "Modeling and Analysis of Power Distribution Networks for Gigabit Applications," *IEEE Transactions on Mobile Computing*, vol. 2, no. 4, pp. 299--313, Oct. 2003.

[54] J. Lee, M. Kim, J. Kim, M. D. Rotaru, and M. K. Iyer, "Reduction of cavity-to-cavity power/ground noise coupling through plane cutout in multilayer PCBs," in *Internationa lSymposium on Electromagnetic Compatibility (EMC 2004)*, vol. 1, Notre Dame, IN, 2004, pp. 35--38vol1.

[55] N. Sankaran, et al., "Coupling noise analysis and high frequency design optimization of power/ground plane stack-up in embedded chip substrate cavities," in *58th Electronic Components and Technology (ECTC 2008) Conference*, 2008, pp. 1874--1879.

[56] G. Antonini, A. C. Scogna, A. Orlandi, and V. Ricchiuti, "Cross-SSN analysis in multilayer printed circuit boards," in *International Symposium on Electromagnetic Compatibility (EMC 2005) Conference*, vol. 3, Santa Barbara, CA, 2005, pp. 705--710Vol3.

[57] K. Bharath, N. Sankaran, A. E. Engin, and M. Swaminathan, "Multi-layer fringe-field augmentations for the efficient modeling of package power planes," in *IEEE Electrical Performance of Electronic Packaging (EPEP) Conference*, San Jose, CA, 2008, pp. 331--334.

[58] J. .-H. Kim, et al., "Electromagnetic modeling and hardware measurements of simultaneous switching noise in high speed systems," in *IEEE International Symposium on Electromagnetic Compatibility (EMC 2002)*, vol. 2, Santa Barbara, CA, 2002, pp. 748--754vol2.

[59] J. Park, et al., "Modeling and measurement of simultaneous switching noise coupling through signal via transition," *IEEE Transactions on Advanced Packaging*, vol. 29, no. 3, pp. 548--559, Aug. 2006.

[60] T. E. Moran, K. L. Virga, G. Aguirre, and J. L. Prince, "Methods to reduce radiation from split ground planes in RF and mixed signal packaging structures," *IEEE Transactions on Advanced Packaging*, vol. 25, no. 3, pp. 409--416, Aug. 2002.

[61] T. H. Kim, J. Lee, H. Kim, and J. Kim, "3 GHz wide frequency model of ferrite bead for power/ground noise simulation of high-speed PCB," in *Electrical Performance of Electronic Packaging (EPEP 2002)*, Monterey, CA, 2002, pp. 217--220.

[62] P. Muthana, E. Matoglu, N. Pham, B. Mutnury, and M. Cases, "Analysis of Embedded Package Capacitors for High Performance Components," in *IEEE Electrical Performance of Electronic Packaging (EPEP 2006)*, Scottsdale, AZ, 2006, pp. 55--58.

[63] J. Choi, V. Govind, and M. Swaminathan, "A novel electromagnetic bandgap (EBG) structure for mixed-signal system applications," in *IEEE Radio and Wireless*

Conference (RAWCON), Atlanta, GA, 2004, pp. 243--246.

[64] K. Bharath, E. Engin, and M. Swaminathan, "Automatic package and board decoupling capacitor placement using genetic algorithms and M-FDM," in *45th ACM/IEEE Design Automation Conference (DAC 2008)*, Anaheim, CA, 2008, pp. 560-565.

[65] Y. Jeong, et al., "Analysis of coupling suppression methods on split power/ground planes using embedded capacitor in multi-layered package," in *54th Electronic Components and Technology Conference*, vol. 1, Las Vegas, NV, 2004, pp. 575--580Vol1.

[66] J. Lee, M. D. Rotaru, M. K. Iyer, H. Kim, and J. Kim, "Analysis and suppression of SSN noise coupling between power/ground plane cavities through cutouts in multilayer packages and PCBs," *IEEE Transactions on Advanced Packaging*, vol. 28, no. 2, pp. 298--309, May 2005.

[67] H. Park, et al., "Co-modeling, Experimental Verification, and Analysis of Chip-Package Hierarchical Power Distribution Network," *IEICE Transactions on Electronics*, vol. E91–C, no. 4, p. 595, Apr. 2008.

[68] R. Panda, S. Sundareswaran, and D. Blaauw, "On the interaction of power distribution network with substrate," in *International Symposium on Low Power Electronics and Design (ISLPED 2001)*, Huntington Beach, CA, 2001, pp. 388--393.

[69] E. Salman, E. G. Friedman, and R. M. Secareanu, "Substrate and Ground Noise Interactions in Mixed-Signal Circuits," in *IEEE International SOC Conference (SOCC)*, Austin, TX, 2006, pp. 293--296.

[70] V. Liberali, R. Rossi, and G. Torelli, "Crosstalk effects in mixed-signal ICs in deep submicron digital CMOS technology," *Microelectronics Journal*, vol. 31, no. 11-12, pp. 893--904, Dec. 2000.

[71] G. Trucco, G. Boselli, and V. Liberali, "An approach to computer simulation of bonding and package crosstalk in mixed-signal CMOS ICs," in *17th Symposium on Integrated Circuits and Systems Design (SBCCI 2004)*, Pernambuco, Brazil, 2004, pp. 129--134.

[72] G. Boselli, et al., "Impact of package parasitics on crosstalk in mixed-signal ICs," in *Proceeding of SPIE vol 5837*, vol. 5837, San Jose, CA, 2005, pp. 213--222.

[73] G. Boselli, et al., "Effects of Package Parasitics on Substrate and Interconnection Crosstalk in Mixed-Signal CMOS ICs," in *Proceedings of wireless reconfigurable terminals and platforms (WiRTeP) Conference*, Rome, Italy, 2006, pp. 90-102.

[74] J. T. Colvin, S. S. Bhatia, and K. K. O, "Effects of substrate resistances on LNA performance and a bondpad," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1339--1344, 1999.

[75] T. Krems, W. H. Haydll, H. Massler, and J. Rudiger, "Advantages of flip chip technology in millimeter-wave packaging," in *IEEE International Microwave Symposium Digest (MTT-S)*, vol. 2, Chennai, India, 1997, pp. 987--990vol2.

[76] T. Krems, A. Tessmann, W. H. Haydl, C. Schmelz, and P. Heide, "Avoiding cross talk and feed back effects in packaging coplanar," in *IEEE International Microwave Symposium Digest (MTT-S)*, vol. 2, 1998, pp. 1091--1094vol2.

[77] T. Krems, W. Haydl, H. Massler, and J. Rudiger, "Millimeter-wave performance of chip interconnections using wire," in *IEEE International Microwave Symposium Digest (MTT-S)*, vol. 1, 1996, pp. 247--250vol1.

[78] A. Ziroff, M. Nalezinki, and W. Menzel, "Improved performance of flip chip assembled MMIC amplifiers on LTCC using a photonic bandgap structure," in *34th European Microwave Conference*, vol. 1, Amsterdam, The Netherlands, 2004, pp. 93--96.

[79] Y. Qian, V. Radisic, and T. Itoh, "Simulation and experiment of photonic band-gap structures for microstrip circuits," in *Proceedings of Asia-Pacific Microwave Conference*, Hong Kong, China, 1997, pp. 585--588.

[80] V. Radisic, Y. Qian, R. Coccioli, and T. Itoh, "Novel 2-D photonic bandgap structure for microstrip lines," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 2, pp. 69--71, 1998.

[81] F. R. Yang, K. P. Ma, Y. Qian, and T. Itoh, "A uniplanar compact photonic-bandgap (UC-PBG) structure and its applications for microwave circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 8, pp. 1509--1514, Aug. 2002.

[82] R. Coccioli, F. R. Yang, K. P. Ma, and T. Itoh, "Aperture-coupled patch antenna on UC-PBG substrate," *IEEE Transactions on Microwave Theory and Techniques*, vol. 47, no. 11, pp. 2123--2130, Nov. 2002.

[83] I. Rumsey, M. Piket-May, and P. K. Kelly, "Photonic bandgap structures used as filters in microstrip circuits," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 10, pp. 336--338, Oct. 2002.

[84] D. Ahn, et al., "A design of the low-pass filter using the novel microstrip defected ground structure," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 1, pp. 86--93, Jan. 2002.

[85] M. L. Her, C. M. Chang, Y. Z. Wang, F. H. Kung, and Y. C. Chiou, "Improved coplanar waveguide (CPW) bandstop filter with photonic bandgap (PBG) structure," *Microwave and Optical Technology Letters*, vol. 38, no. 4, pp. 274--277, Jun. 2003.

[86] V. Radisic, Y. Qian, and T. Itoh, "Broad-band power amplifier using dielectric photonic bandgap structure," *IEEE Microwave and Guided Wave Letters*, vol. 8, no. 1, pp. 13--14, Jan. 2002.

[87] T. Y. Yun and K. Chang, "Uniplanar one-dimensional photonic-bandgap structures and resonators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 3, pp. 549--553, Mar. 2002.

[88] N. C. Karmakar and M. Mollah, "Planar electromagnetic bandgap structures," *International Journal of RF and Microwave Computer-Aided Engineering*, vol. 16, no. 5, pp. 415--429, Sep. 2006.

[89] A. Engin, Y. Toyota, H. T. Kim, and M. Swaminathan, "Analysis and Design of Electromagnetic Bandgap (EBG) Structures for Power Plane Isolation Using 2D Dispersion Diagrams and Scalability," in *IEEE Workshop on Signal Propagation on Interconnects*, Berlin, Germany, 2006, pp. 79-82.

[90] T. Kamgaing and O. M. Ramahi, "A novel power plane with integrated simultaneous switching noise mitigation capability using high impedance surface," *IEEE Microwave and Wireless Components Letters*, vol. 13, no. 1, pp. 21--23, Jan. 2003.

[91] T. Lopetegi, et al., "Novel photonic bandgap microstrip structures using network topology," *Microwave and Optical Technology Letters*, vol. 25, no. 1, pp. 33--36, Apr. 2000.

[92] J. Choi, V. Govind, M. Swaminathan, L. Wan, and R. Doraiswami, "Isolation in mixed-signal systems using a novel electromagnetic bandgap (EBG) structure," in *IEEE 13th Topical Meeting on Electrical Performance of Electronic Packaging*, Portland, OR, 2004, pp. 199--202.

[93] T. L. Wu, Y. H. Lin, T. K. Wang, C. C. Wang, and S. T. Chen, "Electromagnetic bandgap power/ground planes for wideband suppression of ground bounce noise and radiated emission in high-speed circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2935--2942, Sep. 2005.

[94] T. L. Wu, C. C. Wang, Y. H. Lin, T. K. Wang, and G. Chang, "A novel power plane with super-wideband elimination of ground bounce noise on high speed circuits," *IEEE microwave and wireless components letters*, vol. 15, no. 3, pp. 174--176, Mar. 2005.

[95] S. Shahparnia and O. M. Ramahi, "A simple and effective model for electromagnetic bandgap structures embedded in printed circuit boards," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 10, pp. 621--623, Oct. 2005.

[96] T. Kamgaing and O. M. Ramahi, "Design and modeling of high-impedance electromagnetic surfaces for switching noise suppression in power planes," *IEEE Transactions on Electromagnetic Compatibility* , vol. 47, no. 3, pp. 479-489, Aug. 2005.

[97] R. Abhari and G. V. Eleftheriades, "Metallo-dielectric electromagnetic bandgap structures for suppression and isolation of the parallel-plate noise in high-speed circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1629-1639, Jun. 2003.

[98] N. Sankaran, S. Huh, M. Swaminathan, and R. Tummala, "Suppression of vertical coupling using Electromagnetic Band Gap structures," in *IEEE Electrical Performance of Electronic Packaging (EPEP) Conference*, 2008, pp. 173--176.

[99] S. Huh, M. Swaminathan, and F. Muradali, "Design, modeling, and characterization of embedded electromagnetic band gap (EBG) structure," in *IEEE Electrical Performance of Electronic Packaging (EPEP)*, San Jose, CA, 2008, pp. 83--86.

[100] F. Liu, et al., "Chip-last embedded actives and passives in thin organic package for 1--110 GHz multi-band applications," in *Proceedings of the 60th Electronic Components and Technology Conference (ECTC)*, Las Vegas, NV, 2010, pp. 758-763.

[101] Y. Toyota, A. E. Engin, T. H. Kim, M. Swaminathan, and S. Bhattacharya, "Size reduction of electromagnetic bandgap (EBG) structures with new geometries and materials," in *Proceedings of the 56th Electronic Components and Technology Conference*, San Deigo, CA, 2006, p. 6.

[102] S. D. Rogers, "Electromagnetic-bandgap layers for broad-band suppression of TEM modes in power planes," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 8, pp. 2495--2505, Aug. 2005.

[103] J. Choi and M. Swaminathan, "Analysis of alternating impedance electromagnetic bandgap (AI-EBG) structure by transmission line network method," in *Proceedings of the Asia-Pacific Microwave Conference (APMC)*, vol. 3, Suzhou, China, 2006, p. 4.

[104] F. Elek and G. V. Eleftheriades, "A two-dimensional uniplanar transmission-line metamaterial with a negative index of refraction," *New Journal of Physics*, vol. 7, no. 163, p. 163, Aug. 2005.

[105] T. .-L. Wu, Y. .-H. Lin, T. .-K. Wang, C. .-C. Wang, and S. .-T. Chen, "Electromagnetic bandgap power/ground planes for wideband suppression of ground bounce noise and radiated emission in high-speed circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, pp. 2935--2942, Sep. 2005.

[106] Y. Toyota, A. E. Engin, T. H. Kim, and M. Swaminathan, "Stopband analysis using dispersion diagram for two-dimensional electromagnetic bandgap structures in printed circuit boards," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 12, pp. 645--647, Dec. 2006.

[107] R. Remski, "Analysis of photonic bandgap surfaces using Ansoft HFSS," *Microwave Journal*, vol. 43, no. 9, pp. 190--199, Sep. 2000.

[108] S. Shahparnia and O. M. Ramahi, "Electromagnetic interference (EMI) reduction from printed circuit boards (PCB) using electromagnetic bandgap structures," *IEEE Transactions on Electromagnetic Compatibility*, vol. 46, no. 4, pp. 580--587, Nov. 2004.

[109] A. Grbic and G. V. Eleftheriades, "Periodic analysis of a 2-D negative refractive index transmission line structure," *IEEE Transactions on Antennas and Propagation*, vol. 51, no. 10, pp. 2604-1611, Oct. 2003.

[110] J. Choi and M. Swaminathan, "Analysis of alternating impedance electromagnetic bandgap (AI-EBG) structure by transmission line network method," in *Asia-Pacific Conference Proceedings Microwave Conference Proceedings (APMC 2005)*, Long Beach, CA, 2005, p. 4.

[111] Z. Zhang and S. Satpathy, "Electromagnetic wave propagation in periodic structures: Bloch wave solution of Maxwell's equations," *Physical review letters*, vol. 65, no. 21, pp. 2650--2653, Nov. 1990.

[112] T. H. Kim, M. Swaminathan, A. E. Engin, and B. J. Yang, "Electromagnetic Band Gap Synthesis Using Genetic Algorithms for Mixed Signal Applications," *IEEE Transactions on Advanced Packaging*, vol. 32, no. 1, pp. 13-25, Feb. 2009.

[113] H. Zhang and K. J. Chen, "A tri-section stepped-impedance resonator for cross-coupled bandpass filters," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 6, pp. 401-403, Jun. 2005.

[114] M. Makimoto and S. Yamashita, "Bandpass Filters Using Parallel Coupled Stripline Stepped Impedance Resonators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 28, no. 12, pp. 1413--1417, Dec. 1980.

[115] C. F. Chen, T. Y. Huang, C. P. Chou, and R. B. Wu, "Microstrip diplexers design with common resonator sections for compact size, but high isolation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 5, pp. 1945--1952, May 2006.

[116] A. Griol, D. Mira, J. Marti, and J. L. Corral, "Microstrip side-coupled ring bandpass filters with mode coupling control for harmonic suppression," *Electronics Letters*, vol. 40, no. 15, pp. 943--945, Jul. 2004.

[117] H. .-W. Wu, et al., "Design of a compact microstrip triplexer for multiband applications," in *European Microwave Conference*, Munich, Germany, 2007, pp. 834-837.

[118] M. Sagawa, M. Makimoto, and S. Yamashita, "Geometrical structures and fundamental characteristics of microwave stepped-impedance resonators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 45, no. 7, pp. 1078-1085, Jul. 1997 .

[119] K. S. Chin, J. H. Yeh, and S. H. Chao, "Compact dual-band bandstop filters using stepped-impedance resonators," *IEEE Microwave and Wireless Components Letters*, vol. 17, no. 12, pp. 849--851, Dec. 2007.

[120] D. M. Pozar, "Microwave Engineering, 2nd ed.," in *Microwave Engineering, 2nd ed.* New York: Wiley, 1998, pp. 143-146.

[121] E. Engin, et al., "Finite-difference modeling of noise coupling between power/ground planes in multilayered packages and boards," in *Proceedings of the 56th Electronic Components and Technology Conference (ECTC)*, San Diego, CA, 2006, pp. 1262-1267.

[122] Y. Toyota, A. E. Engin, T. H. Kim, M. Swaminathan, and K. Uriu, "Stopband prediction with dispersion diagram for electromagnetic bandgap structures in printed circuit boards," in *IEEE International Symposium on Electromagnetic Compatibility, 2006* , Portland, 2006, pp. 807-811.

[123] J. Choi, V. Govind, R. Mandrekar, S. Janagama, and M. Swaminathan, "Noise reduction and design methodology in mixed-signal systems with alternating impedance electromagnetic bandgap (AI-EBG) structure," in *IEEE International Microwave Symposium Digest (IMS)*, Long Beach, CA, 2005, p. 4.

[124] J. Lin, "Chip-Package Codesign for High-Frequency Circuits and Systems," *IEEE Micro*, vol. 18, no. 4, pp. 24-32, Jul. 1998.

[125] W. Kim, et al., "Electrical design of wafer level package on board for gigabit data transmission," in *5th Conference on Electronics Packaging Technology (EPTC 2003)* , Singapore, 2003 , pp. 150-159.

[126] A. Jentzsch and W. Heinrich, "Theory and measurements of flip-chip interconnects for frequencies up to 100 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 5, pp. 871-878, May 2001 .

[127] R. D.Pendse, "Flip Chip Interconnection Pad Layout," USA Hardware 7,605,480 B2, Oct. 20, 2009.

[128] IC Interconnect. [Online]. http://www.icinterconnect.com/design.htm (June 7th, 2010)

[129] I. Corporation. (1999, Feb.) Design For EMI: Application Note - 589. [Online]. http://www.intel.com/design/pentiumii/applnots/24333402.PDF (August 9th, 2010)

[130] A. K. Verma and E. K. Sharma, "Analysis and circuit model of a multilayer semiconductor slow-wave microstrip line," *IEE Proceedings of Microwaves, Antennas and Propagation*, vol. 151, no. 5, pp. 441--449, Oct. 2004.

[131] V. Milanovic, et al., "Characterization of broad-band transmission for coplanar waveguides on CMOS silicon substrates," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 5, pp. 632--640, May 1998.

[132] H. Hasegawa, M. Furukawa, and H. Yanai, "Properties of microstrip line on Si-SiO2 system," *IEEE Transactions on Microwave Theory and Techniques*, vol. 19, no. 11, pp. 869--881, Nov. 1971.

[133] J. P. Raskin, A. Viviani, D. Flandre, and J. P. Colinge, "Substrate crosstalk reduction using SOI technology," *IEEE Transactions on Electron Devices*, vol. 44, no. 12, pp. 2252--2261, Dec. 1997.

[134] R. Gharpurey and E. Charbon, "Substrate coupling: Modeling, simulation and design perspectives," in *Proceedings of 5th International Symposium on Quality Electronic Design*, San Jose, CA, 2004, pp. 283--290.

[135] Y. R. Kwon, V. M. Hietala, and K. S. Champlin, "Quasi-TEM analysis of "slow-wave" mode propagation on coplanar microstructure MIS transmission lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 35, no. 6, pp. 545-551, Jun. 1987.